Compal Confidential

PEW71_81_91 UMA <LA-6582P> M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M

2010-06-18
REV:0.2

Security Classification	Compal Secret Data		
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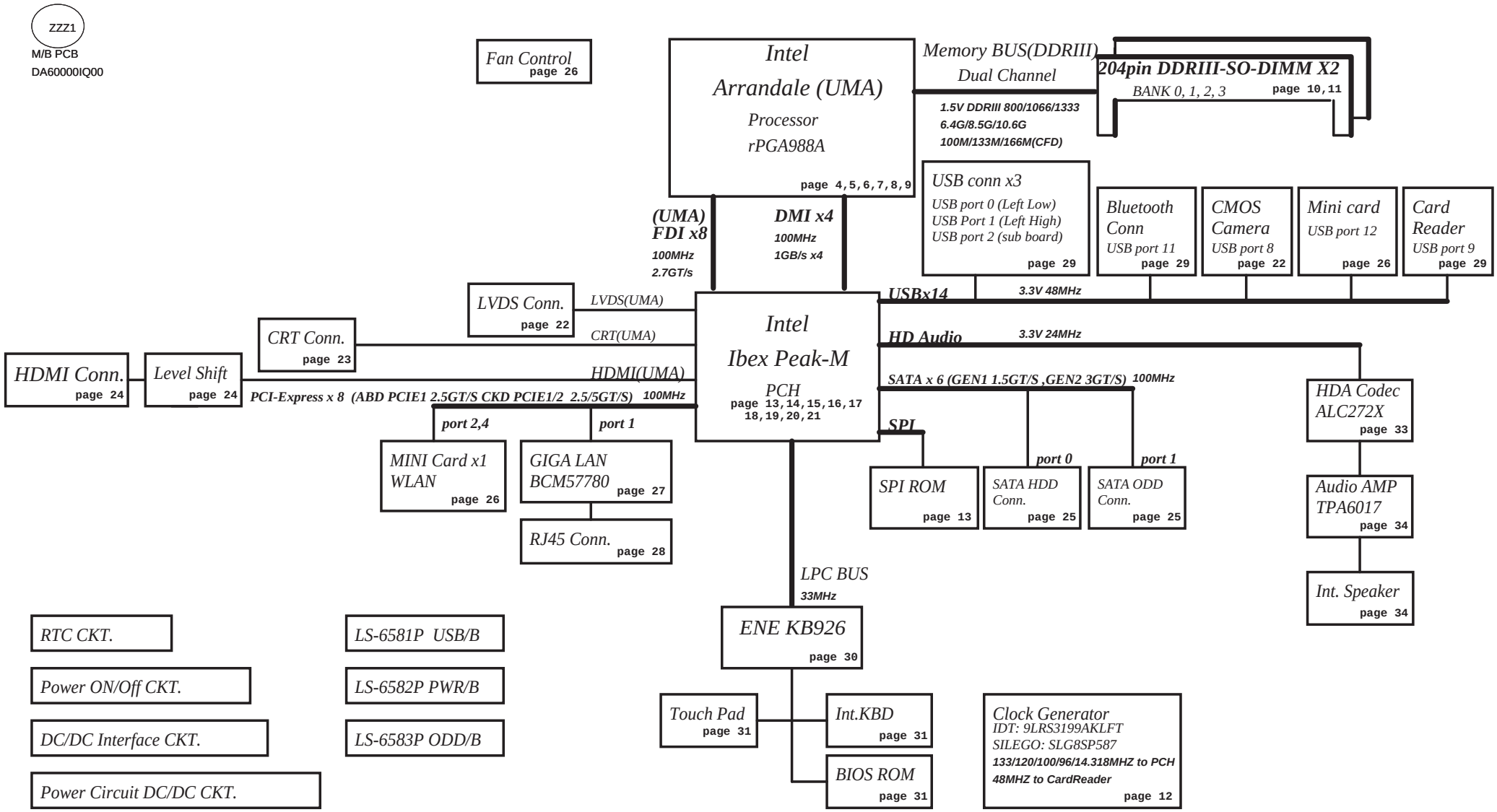
Model Name PEW71_81 UMA
File Name : LA-6582P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.05VS_VTT	1.05V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Project ID / Board ID Table for EC-AD channel

Vcc	3.3V +/- 5%
Ra/Rc	100K +/- 5%

	Rb / Rd	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Board ID	Project ID
0	0	0 V	0 V	0 V	0.1	Original NEW70/80/90/50/71/91
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	0.2	PEW71/81/91 Audio Mono/Crystal
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	0.3	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	1.0	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V		
5	100K +/- 5%	1.453 V	1.650 V	1.759 V		
6	200K +/- 5%	1.935 V	2.200 V	2.341 V		PEW71/81/91 Audio Mono/SUSCLK
7	NC	2.500 V	3.300 V	3.300 V		NEW71/91 Optumis

BTO Option Table

BTO Item	BOM Structure
HDMI	HDMI@

USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port	3 External USB Port
EHCI1	UHCI0	0	Ext1 Left Low USB	Ext1 Left Low USB
		1	Ext2 Left High USB	Ext2 Left High USB
	UHCI1	2	Ext3 Right USB	Ext3 Right USB
		3		
	UHCI2	4		
		5		
	UHCI3	6		
		7		
EHCI2	UHCI4	8	Camera	Camera
		9	Card Reader	Card Reader
	UHCI5	10		
		11	Blue Tooth	Blue Tooth
	UHCI6	12	1st Min-Card	1st Min-Card
		13		

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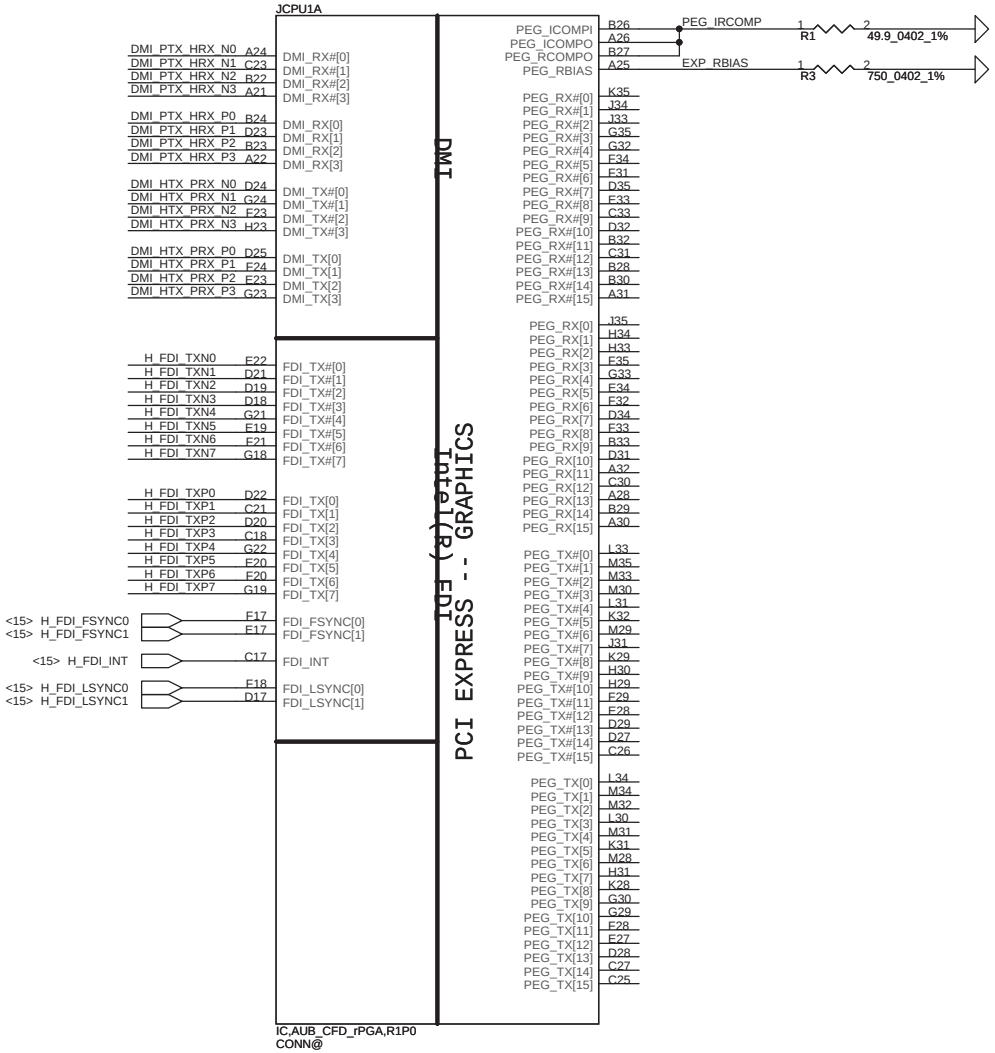

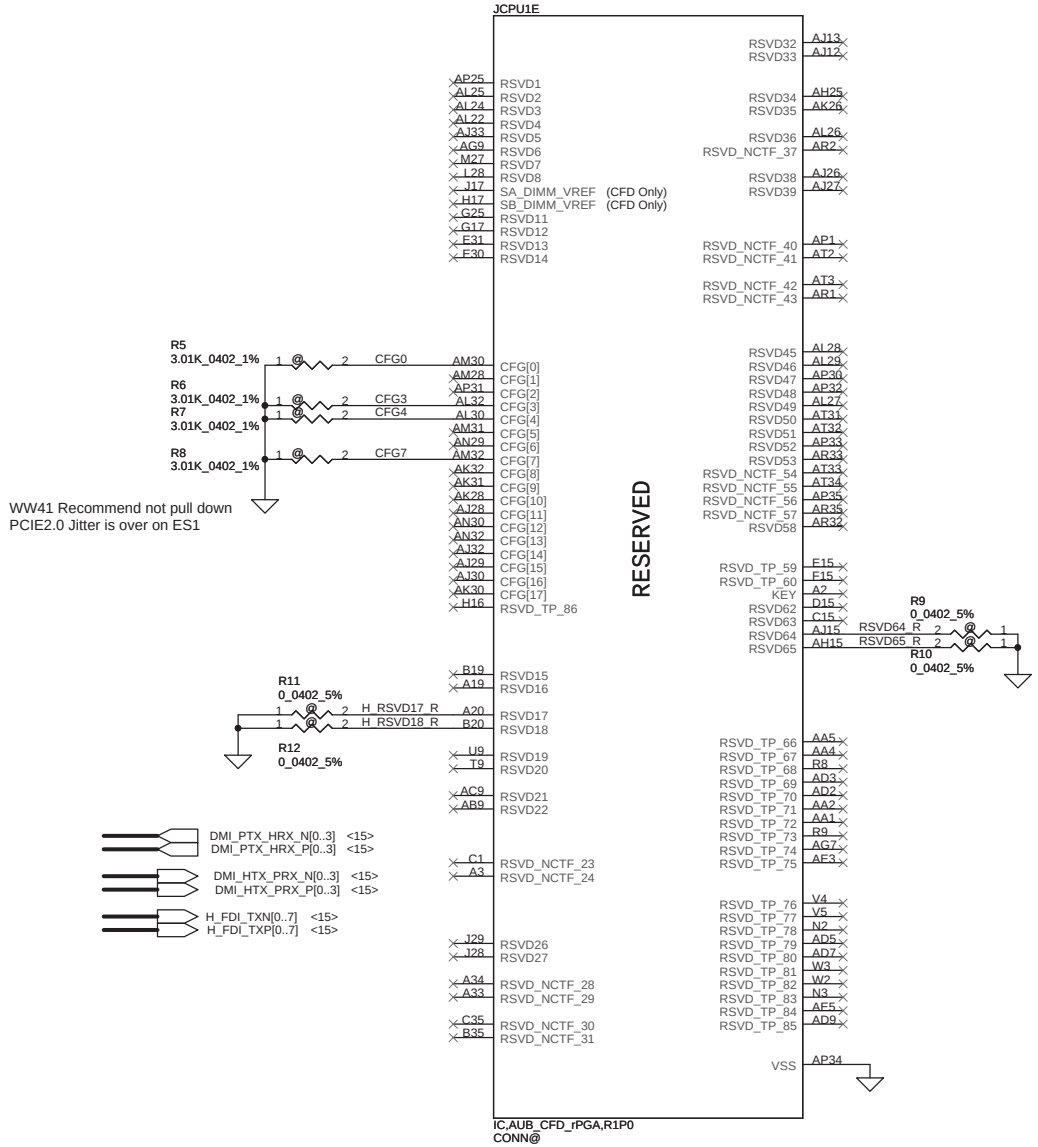

eDP Signals Mapping

eDP Singal	PEG Singals	Lane Reversal
eDP_TX0	PEG_HTX_C_GRX_P15	PEG_HTX_C_GRX_P0
eDP_TX#0	PEG_HTX_C_GRX_N15	PEG_HTX_C_GRX_N0
eDP_TX1	PEG_HTX_C_GRX_P14	PEG_HTX_C_GRX_P1
eDP_TX#1	PEG_HTX_C_GRX_N14	PEG_HTX_C_GRX_N1
eDP_TX2	PEG_HTX_C_GRX_P13	PEG_HTX_C_GRX_P2
eDP_TX#2	PEG_HTX_C_GRX_N13	PEG_HTX_C_GRX_N2
eDP_TX3	PEG_HTX_C_GRX_P12	PEG_HTX_C_GRX_P3
eDP_TX#3	PEG_HTX_C_GRX_N12	PEG_HTX_C_GRX_N3
eDP_AUX	PEG_GTX_C_HRX_P13	PEG_GTX_C_HRX_P2
eDP_AUX#	PEG_GTX_C_HRX_N13	PEG_GTX_C_HRX_N2
eDP_HPD#	PEG_GTX_C_HRX_P12	PEG_GTX_C_HRX_P3

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CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

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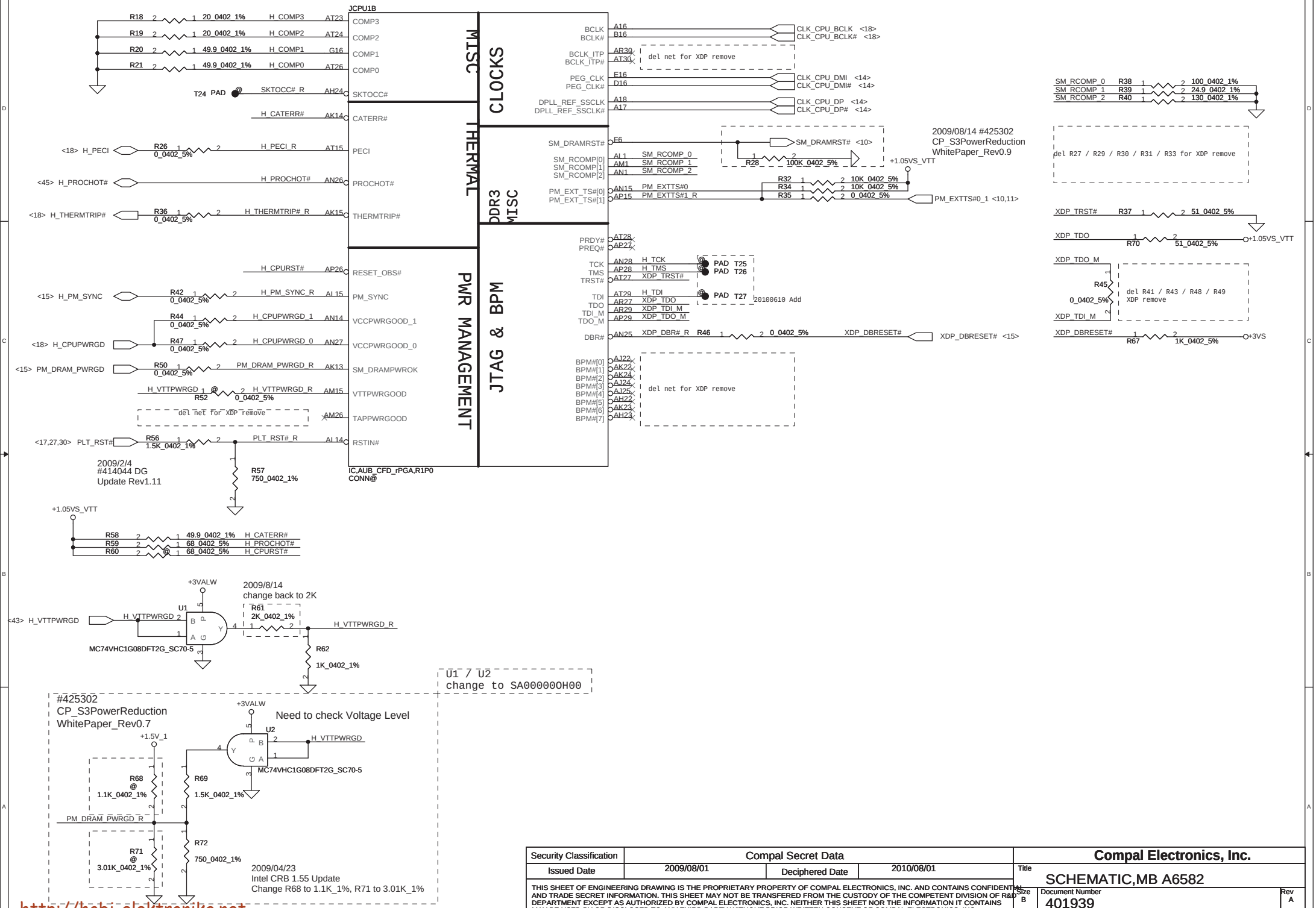

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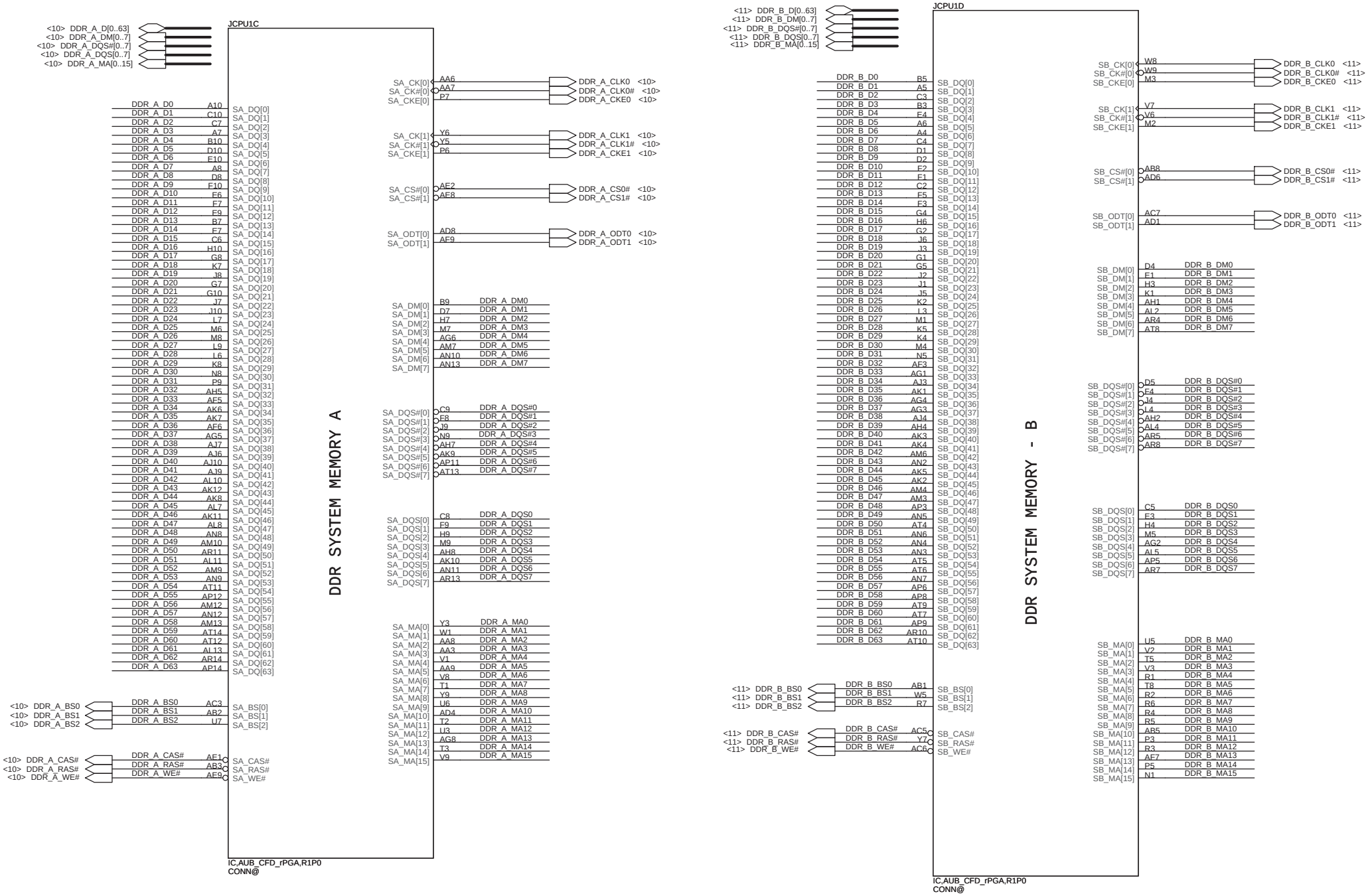

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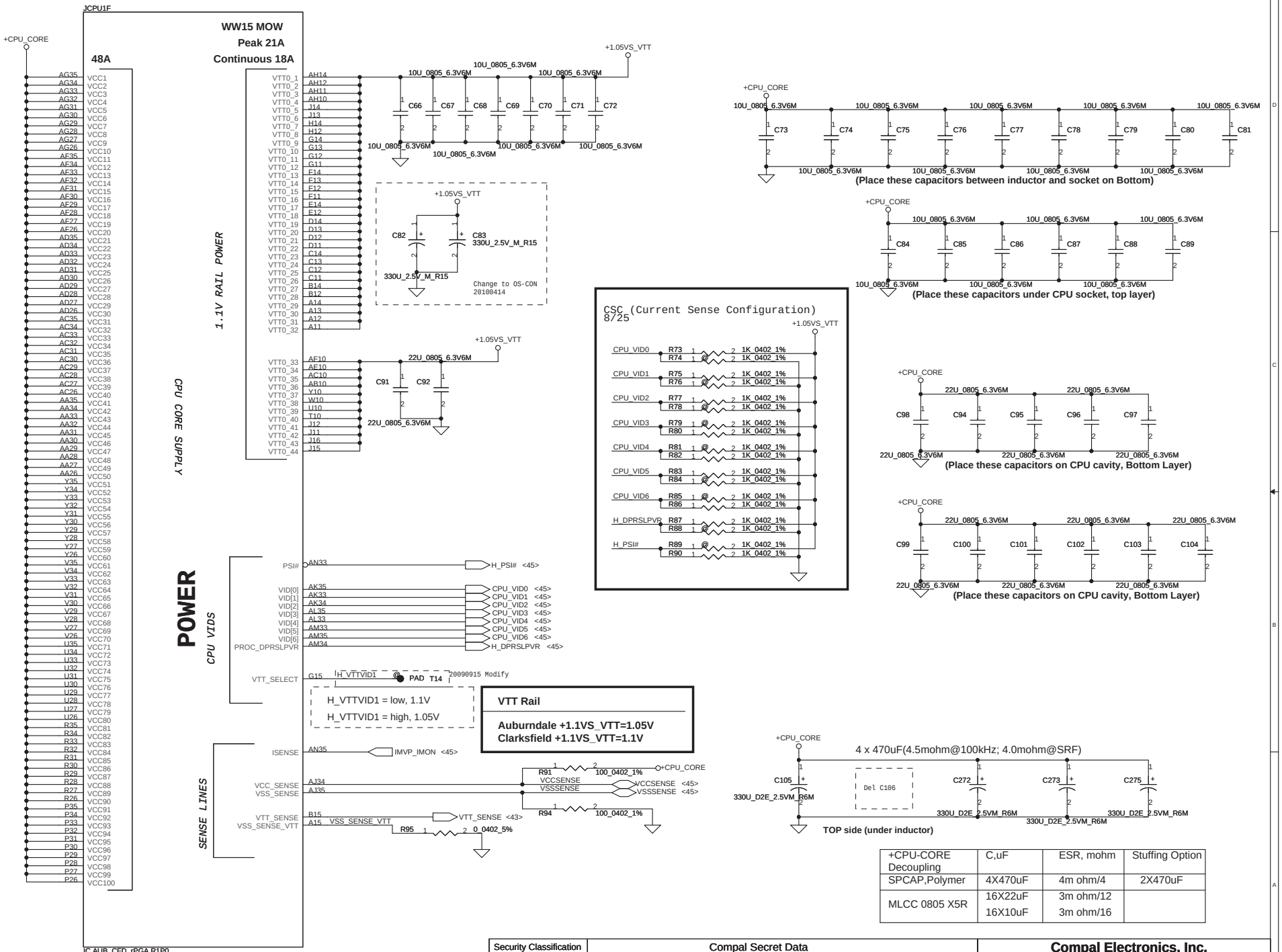

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF 16X10uF	3m ohm/12 3m ohm/16	

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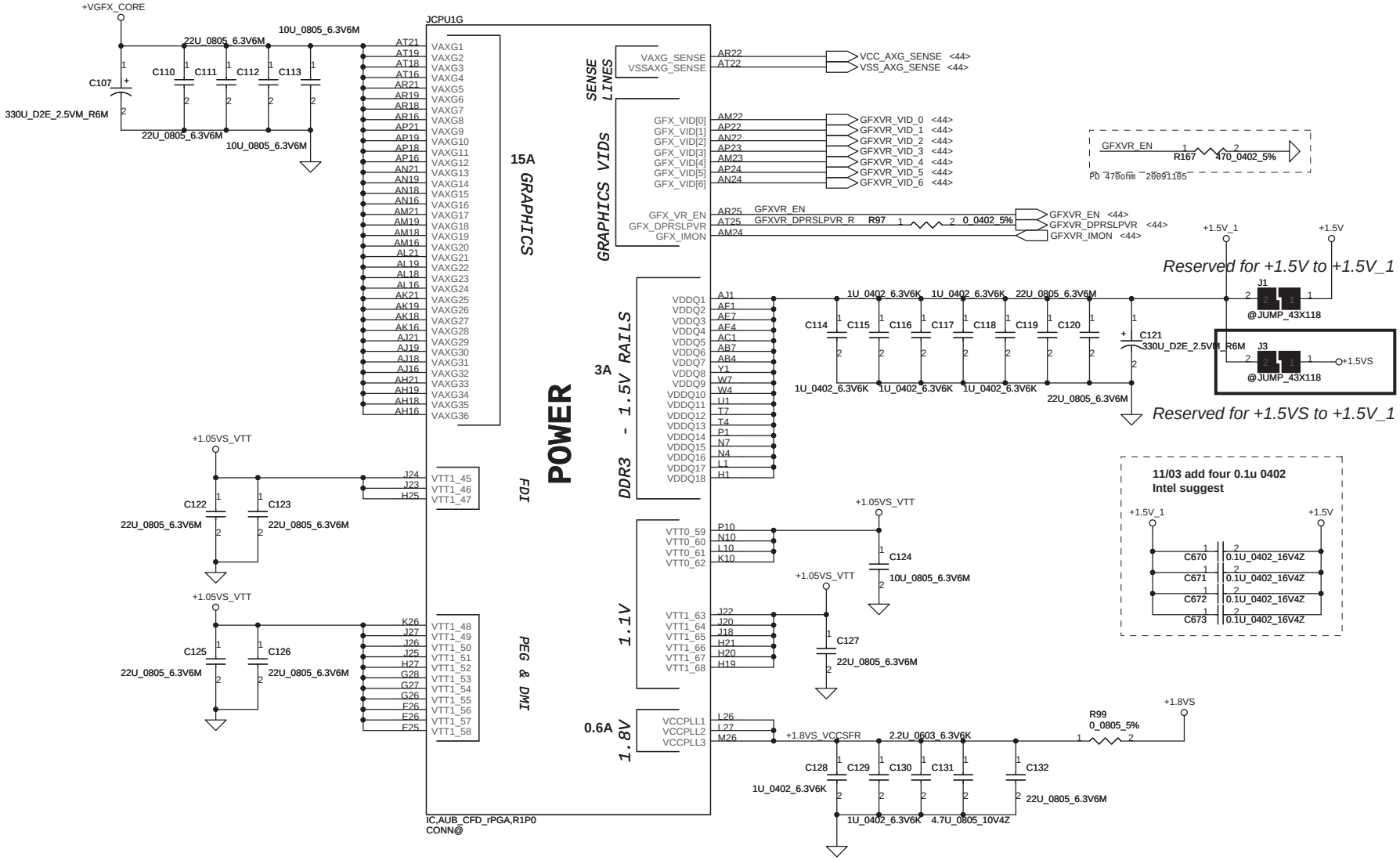

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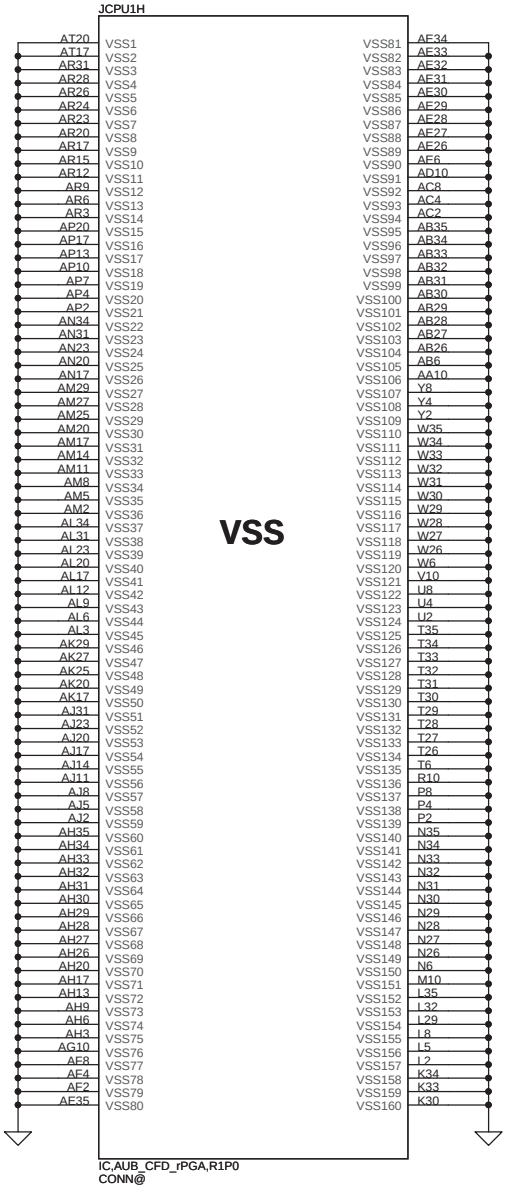

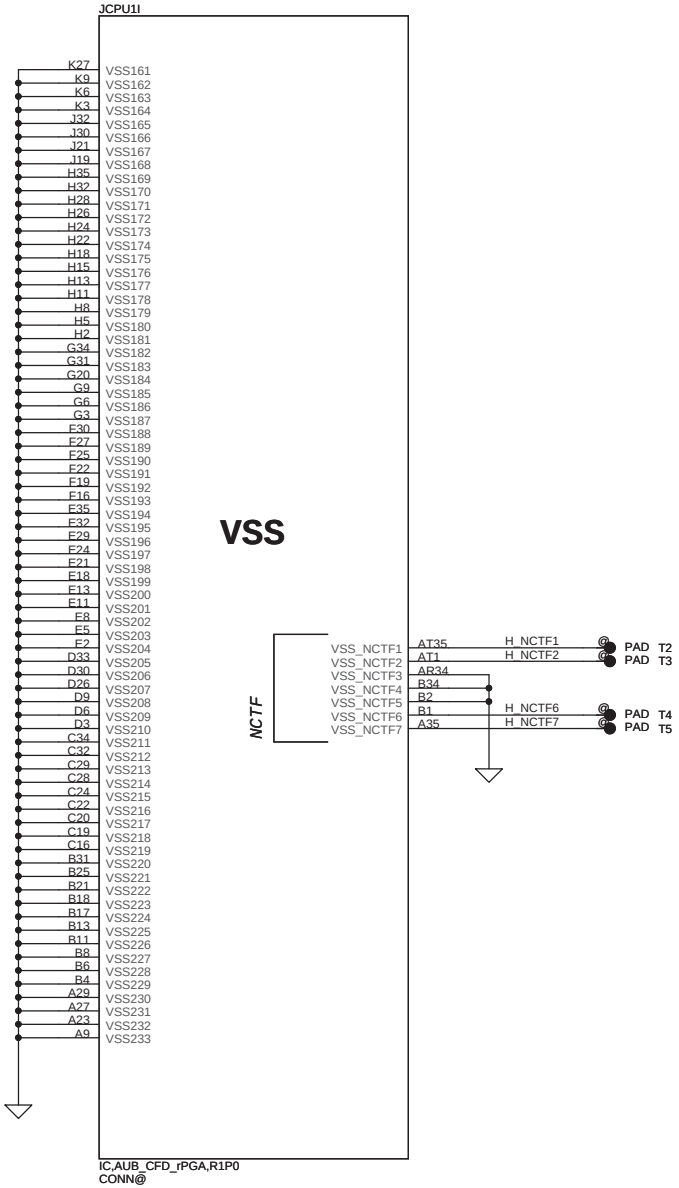

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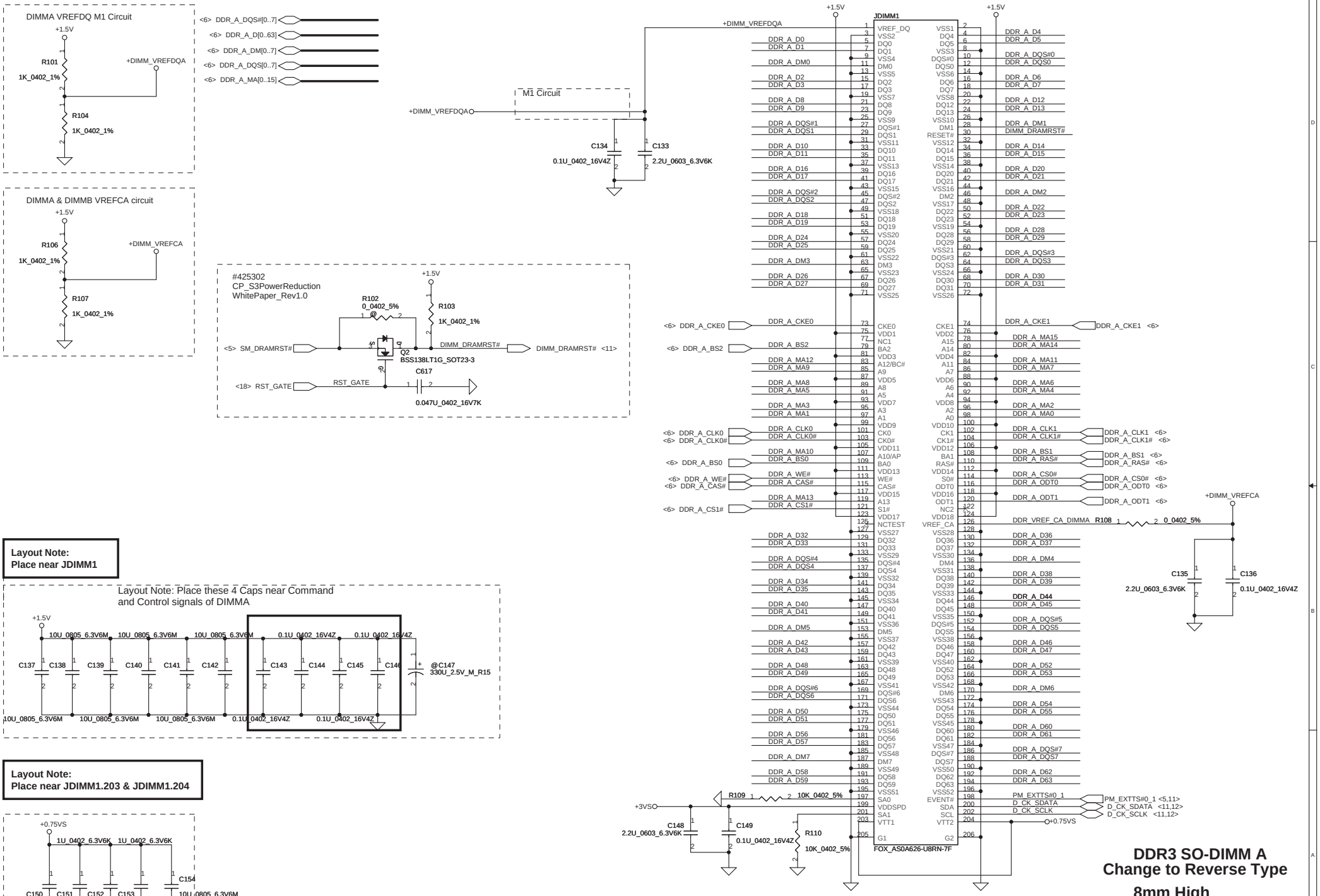

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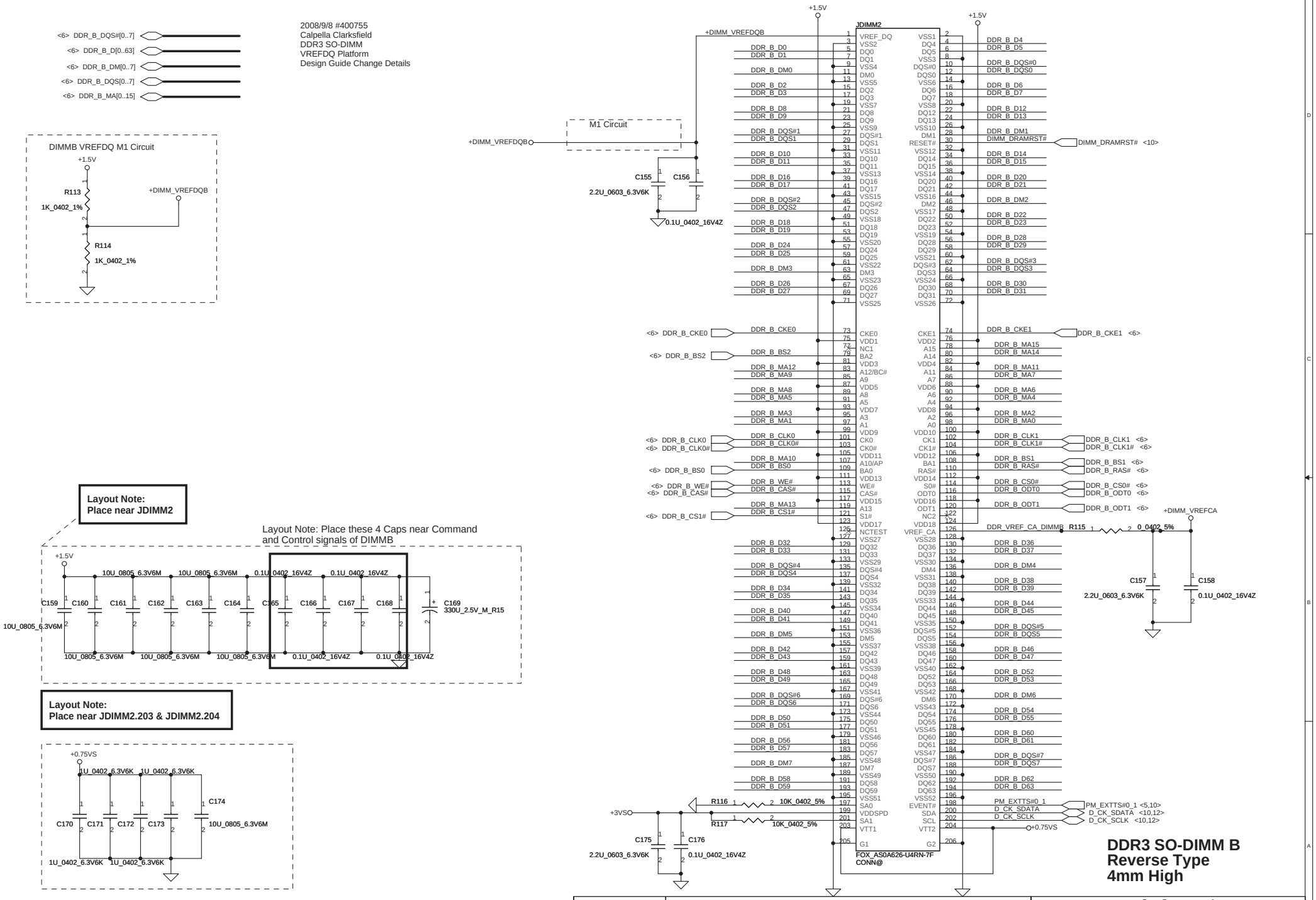

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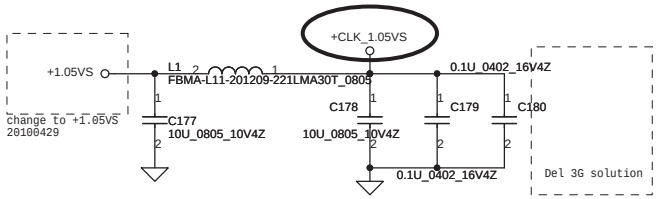
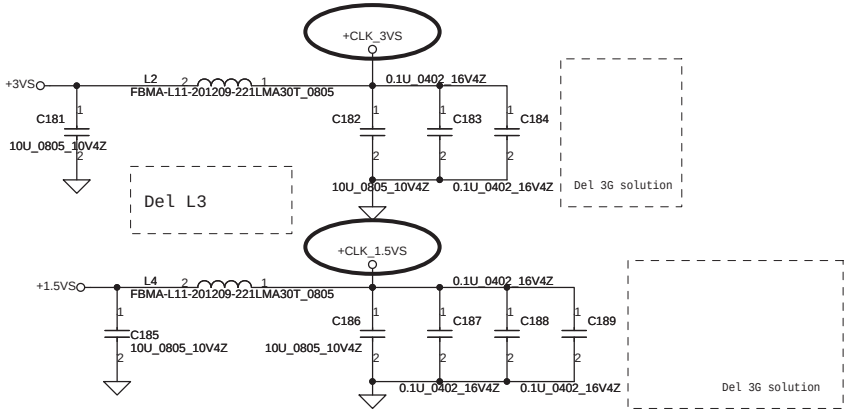
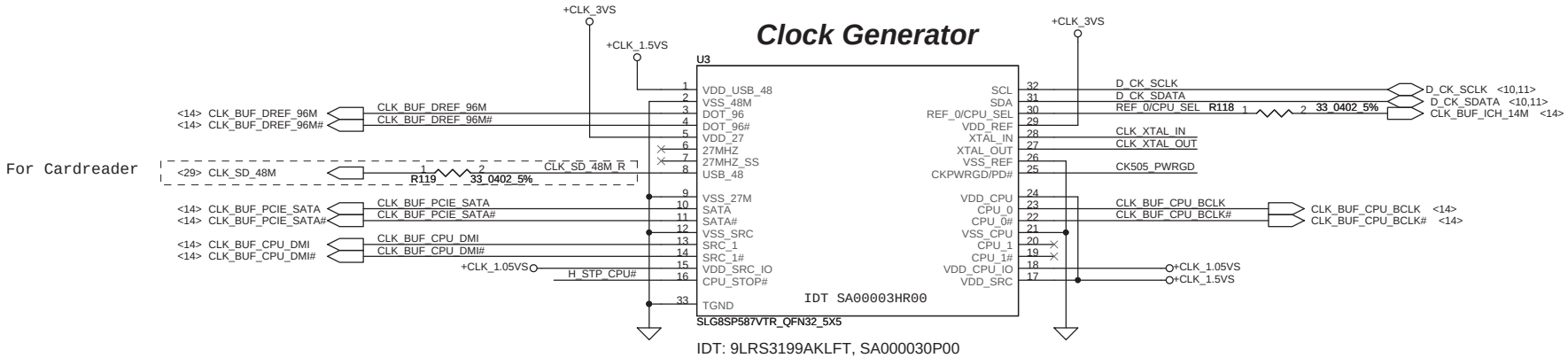




Clock Generator



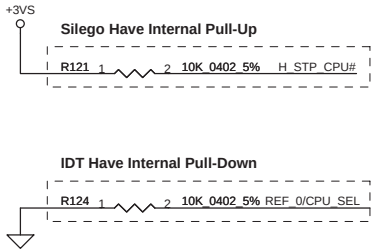
IDT: 9LRS3199AKLFT, SA000030P00

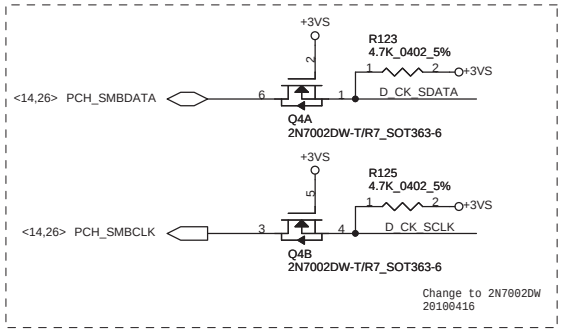
SILEGO: SLG8SP587V(WF), SA00002XY10

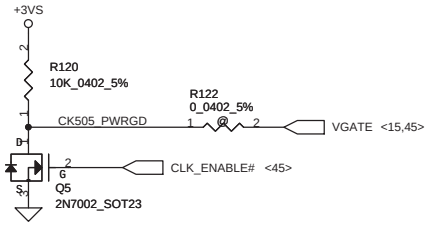
Low Power:

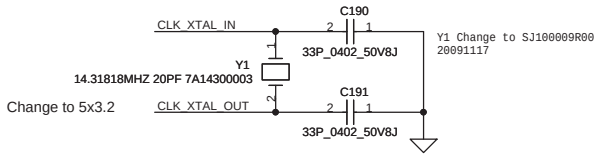
IDT: 9LVS3199AKLFT, SA00003HR00

Realtek: RTM890N-631-GRT, SA00003HQ00









PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

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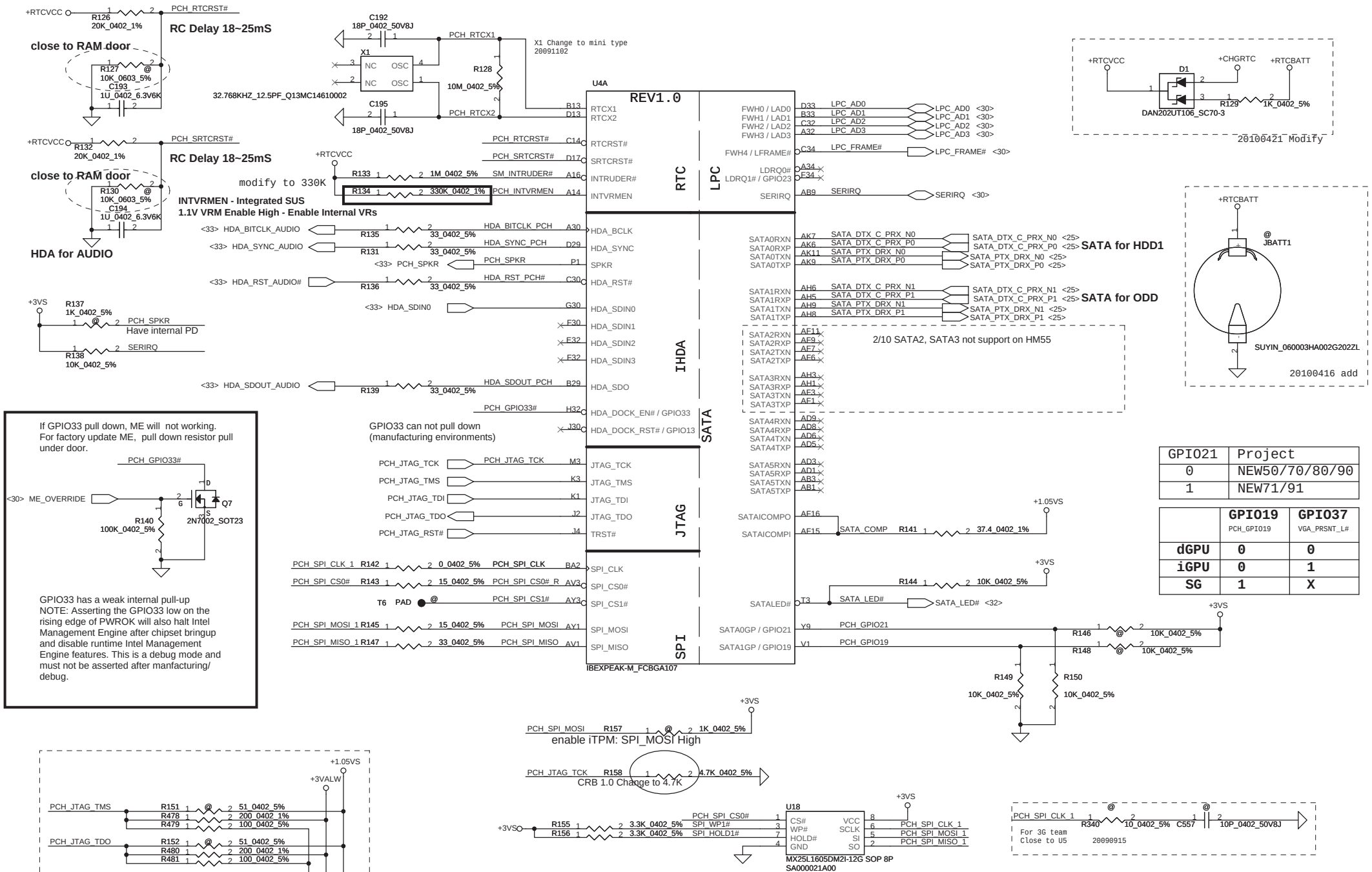

GPIO21	Project
0	NEW50/70/80/90
1	NEW71/91

	GPIO19 PCH_GPIO19	GPIO37 VGA_PRSNT_L#
dGPU	0	0
iGPU	0	1
SG	1	X

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1. Connect Directly
   EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS
   CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS
   LAN
4. Level Shift3, Pull-Up to +3VS
   CPU & PCH XDP

U4B

REV1.0

PCI-E*

For PCIE LAN

<27> PCIE_DTX_C_PRX_N1 — PCIE_DTX_C_PRX_N1 BG30 — PERN1
<27> PCIE_DTX_C_PRX_P1 — PCIE_DTX_C_PRX_P1 BJ30 — PERP1
<27> PCIE_PTX_C_DRX_N1 — C197 0.1U_0402_16V7K — PCIE_PTX_DRX_N1 BF29 — PETN1
<27> PCIE_PTX_C_DRX_P1 — C198 0.1U_0402_16V7K — PCIE_PTX_DRX_P1 BH29 — PETP1

For Wireless LAN

<26> PCIE_DTX_C_PRX_N2 — PCIE_DTX_C_PRX_N2 AW30 — PERN2
<26> PCIE_DTX_C_PRX_P2 — PCIE_DTX_C_PRX_P2 BA30 — PERP2
<26> PCIE_PTX_C_DRX_N2 — C199 0.1U_0402_16V7K — PCIE_PTX_DRX_N2 BC30 — PETN2
<26> PCIE_PTX_C_DRX_P2 — C200 0.1U_0402_16V7K — PCIE_PTX_DRX_P2 BD30 — PETP2

AU30 PERN3
AT30 PERP3
AU32 PETN3
AV32 PETP3

BA32 PERN4
BB32 PERP4
BD32 PETN4
BE32 PETP4

BF33 PERN5
BH33 PERP5
BG32 PETN5
BJ32 PETP5

BA34 PERN6
AW34 PERP6
BC34 PETN6
BD34 PETP6

2/10 PCIE7, PCIE8 not support on HM55

AT34 PERN7
AU34 PERP7
AU36 PETN7
AV36 PETP7

BG34 PERN8
BJ34 PERP8
BG36 PETN8
BJ36 PETP8

For PCIE LAN

<27> CLK_PCIE_LAN# — AK48 — CLKOUT_PCIE0N
<27> CLK_PCIE_LAN — AK47 — CLKOUT_PCIE0P

<27> LAN_CLKREQ# — R164 0_0402_5% — PCH_GPIO73 — P9 — PCIECLKRQ0# / GPIO73

For Wireless LAN

<26> CLK_PCIE_MINI1# — AM43 — CLKOUT_PCIE1N
<26> CLK_PCIE_MINI1 — AM45 — CLKOUT_PCIE1P

<26> MINI1_CLKREQ# — R165 0_0402_5% — PCH_GPIO18 — U4 — PCIECLKRQ1# / GPIO18

AM47 CLKOUT_PCIE2N
AM48 CLKOUT_PCIE2P

PCH_GPIO20 — N4 — PCIECLKRQ2# / GPIO20

AH42 CLKOUT_PCIE3N
AH41 CLKOUT_PCIE3P

PCH_GPIO25 — A8 — PCIECLKRQ3# / GPIO25

AM51 CLKOUT_PCIE4N
AM53 CLKOUT_PCIE4P

PCH_GPIO26 — M9 — PCIECLKRQ4# / GPIO26

AJ50 CLKOUT_PCIE5N
AJ52 CLKOUT_PCIE5P

PCH_GPIO44 — H6 — PCIECLKRQ5# / GPIO44

AK53 CLKOUT_PEG_B_N
AK51 CLKOUT_PEG_B_P

PCH_GPIO56 — P13 — PEG_B_CLKRQ# / GPIO56

IBEXPEAK-M_FCBGA107

SMBus

SMBALERT# / GPIO11 — B9 — EC_LID_OUT# — EC_LID_OUT# <30>
SMBCLK — H14 — PCH_SMBCLK — PCH_SMBCLK <12,26>
SMBDATA — C8 — PCH_SMBDATA — PCH_SMBDATA <12,26>
SML0ALERT# / GPIO60 — J14 — PCH_GPIO60
SML0CLK — C6
SML0DATA — G8
SML1ALERT# / GPIO74 — M14 — PCH_GPIO74
SML1CLK / GPIO58 — E10 — PCH_SML1CLK
SML1DATA / GPIO75 — G12 — PCH_SML1DAT

Controller Link

CL_CLK1 — T13
CL_DATA1 — T11
CL_RST1# — T9

PEG

PEG_A_CLKRQ# / GPIO47 — H1 — PEG_CLKREQ#

+3VALW — R159 10K_0402_5% — 20090915 Add

CLKOUT_PEG_A_N — AD43
CLKOUT_PEG_A_P — AD45

CLKOUT_DMI_N — AN4 — CLK_CPU_DMI# <5>
CLKOUT_DMI_P — AN2 — CLK_CPU_DMI <5>

From CLK BUFFER

CLKOUT_DP_N / CLKOUT_BCLK1_N — AT1 — CLK_CPU_DP# <5>
CLKOUT_DP_P / CLKOUT_BCLK1_P — AT3 — CLK_CPU_DP <5>

CLKIN_DMI_N — AW24 — CLK_BUF_CPU_DMI# <12>
CLKIN_DMI_P — BA24 — CLK_BUF_CPU_DMI <12>

CLKIN_BCLK_N — AP3 — CLK_BUF_CPU_BCLK# <12>
CLKIN_BCLK_P — AP1 — CLK_BUF_CPU_BCLK <12>

CLKIN_DOT_96N — F18 — CLK_BUF_DREF_96M# <12>
CLKIN_DOT_96P — E18 — CLK_BUF_DREF_96M <12>

CLKIN_SATA_N / CKSSCD_N — AH13 — CLK_BUF_PCIE_SATA# <12>
CLKIN_SATA_P / CKSSCD_P — AH12 — CLK_BUF_PCIE_SATA <12>

REFCLK14IN — P41 — R338 10_0402_5% — C555 10P_0402_50V8J — CLK_BUF_ICH_14M <12>

CLKIN_PCILOOPBACK — J42 — CLK_PCI_FB <17>

XTAL25_IN — AH51 — XTAL25_IN
XTAL25_OUT — AH53 — XTAL25_OUT

XCLK_RCOMP — AF38 — XCLK_RCOMP — R169 90.9_0402_1% — +1.05VS

Clock Flex

CLKOUTFLEX0 / GPIO64 — T45
CLKOUTFLEX1 / GPIO65 — P43 — PROJECT_ID1 — R171 10K_0402_5%
CLKOUTFLEX2 / GPIO66 — T42 — PROJECT_ID0 — @R172 10K_0402_5% — @R174 10K_0402_5%
CLKOUTFLEX3 / GPIO67 — N50 — R175 10K_0402_5%

Project Port ID

+3VS

6/9 MOW23 Request add 25MHz crystal supporting Integrated Graphics

C203 27P_0402_50V8J
R170 1M_0402_5%
Y2 25MHZ_20PF_7A25000012
C204 27P_0402_50V8J
Change to 5x3.2

+3VS
MINI1_CLKREQ# — R177 10K_0402_5%
PCH_GPIO20 — R178 10K_0402_5%

+3VALW
EC_LID_OUT# — R179 10K_0402_5%
PCH_SMBCLK — R180 2.2K_0402_5%
PCH_SMBDATA — R181 2.2K_0402_5%
PCH_GPIO60 — R182 10K_0402_5%
PCH_SML1CLK — R183 2.2K_0402_5%
PCH_SML1DAT — R184 2.2K_0402_5%
PCH_GPIO74 — R185 10K_0402_5%
PCH_GPIO44 — R187 10K_0402_5%
PCH_GPIO56 — R188 10K_0402_5%
PCH_GPIO73 — R189 10K_0402_5%

+3VALW
2009/09/23:Change to +3VALW
PCH_GPIO26 — R166 10K_0402_5%
PCH_GPIO25 — R186 10K_0402_5%
2009/08/13: Change back to +3VALW

0602 GPIO65 no use
PULL HIGH:PVT
PULL DOWN:DVT

GPIO66 6L/8L SATA register separe		
GPIO66	0	6L *
	1	8L

+3VS
PCH_SML1CLK — 2N7002DW-T/R7_SOT363-6 Q9A — EC_SMB_CK2 — EC_SMB_CK2 <30>

+3VS
Pull high +3VS at KB926 side
PCH_SML1DAT — 2N7002DW-T/R7_SOT363-6 Q9B — EC_SMB_DA2 — EC_SMB_DA2 <30>

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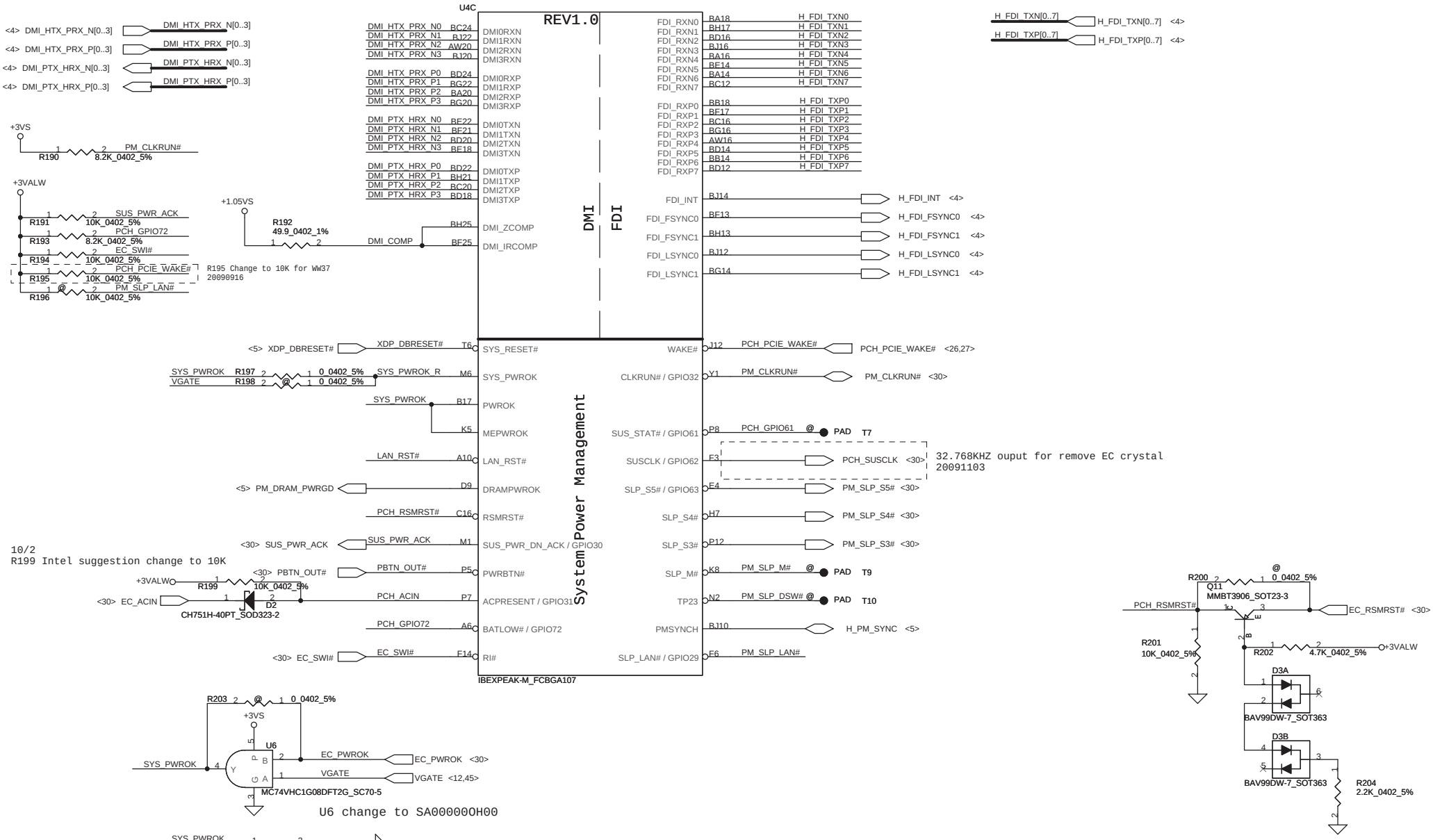

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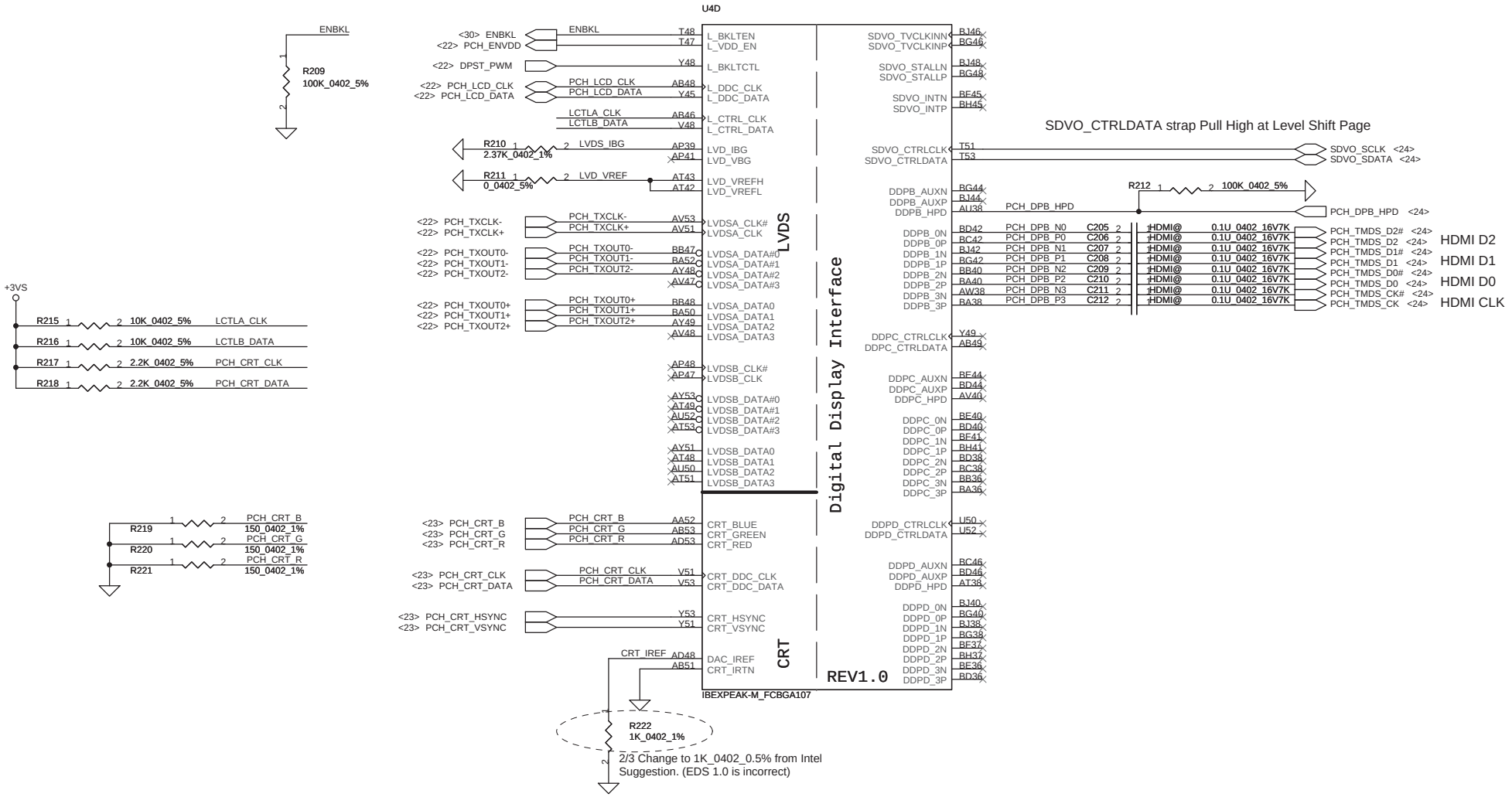

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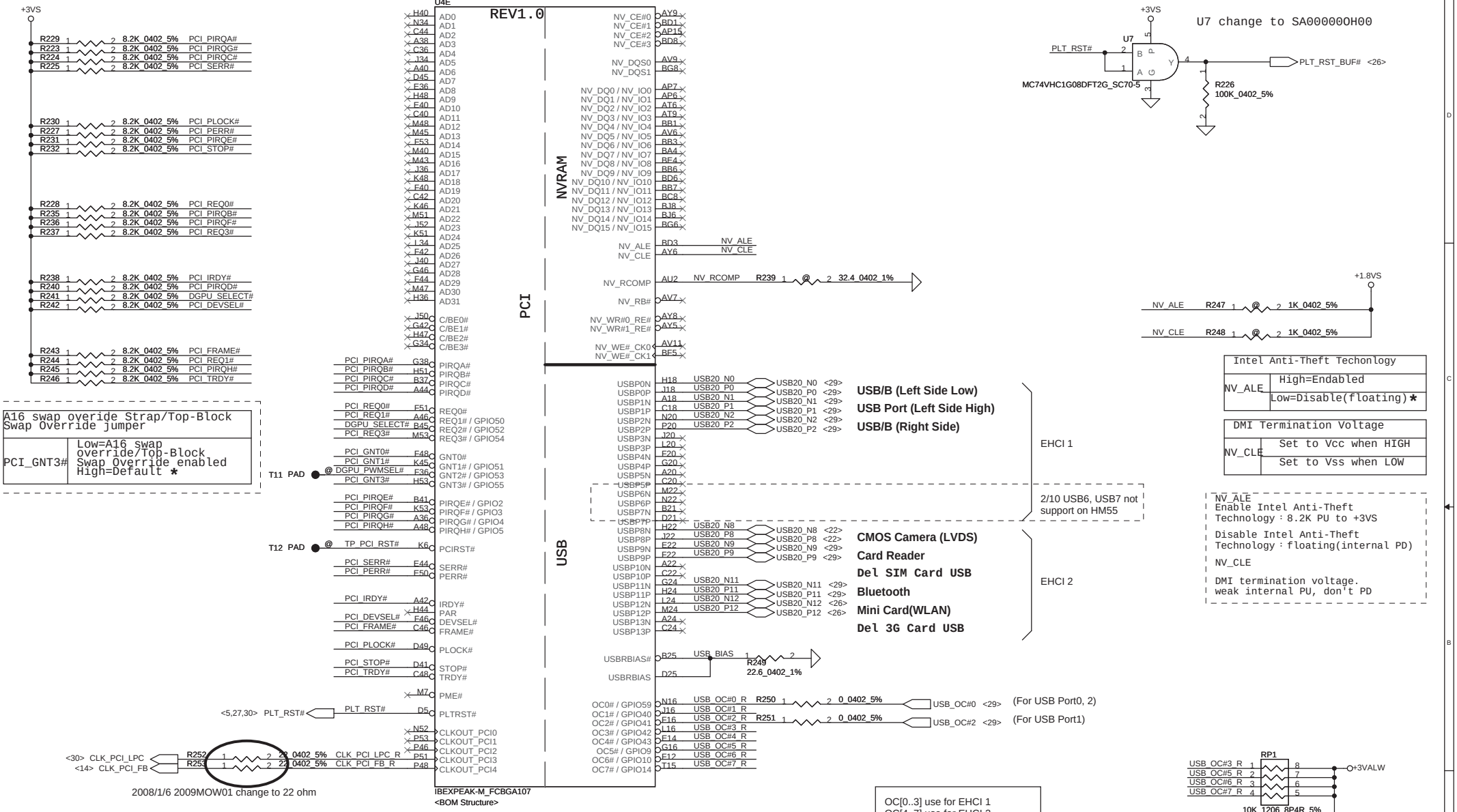

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
* 1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

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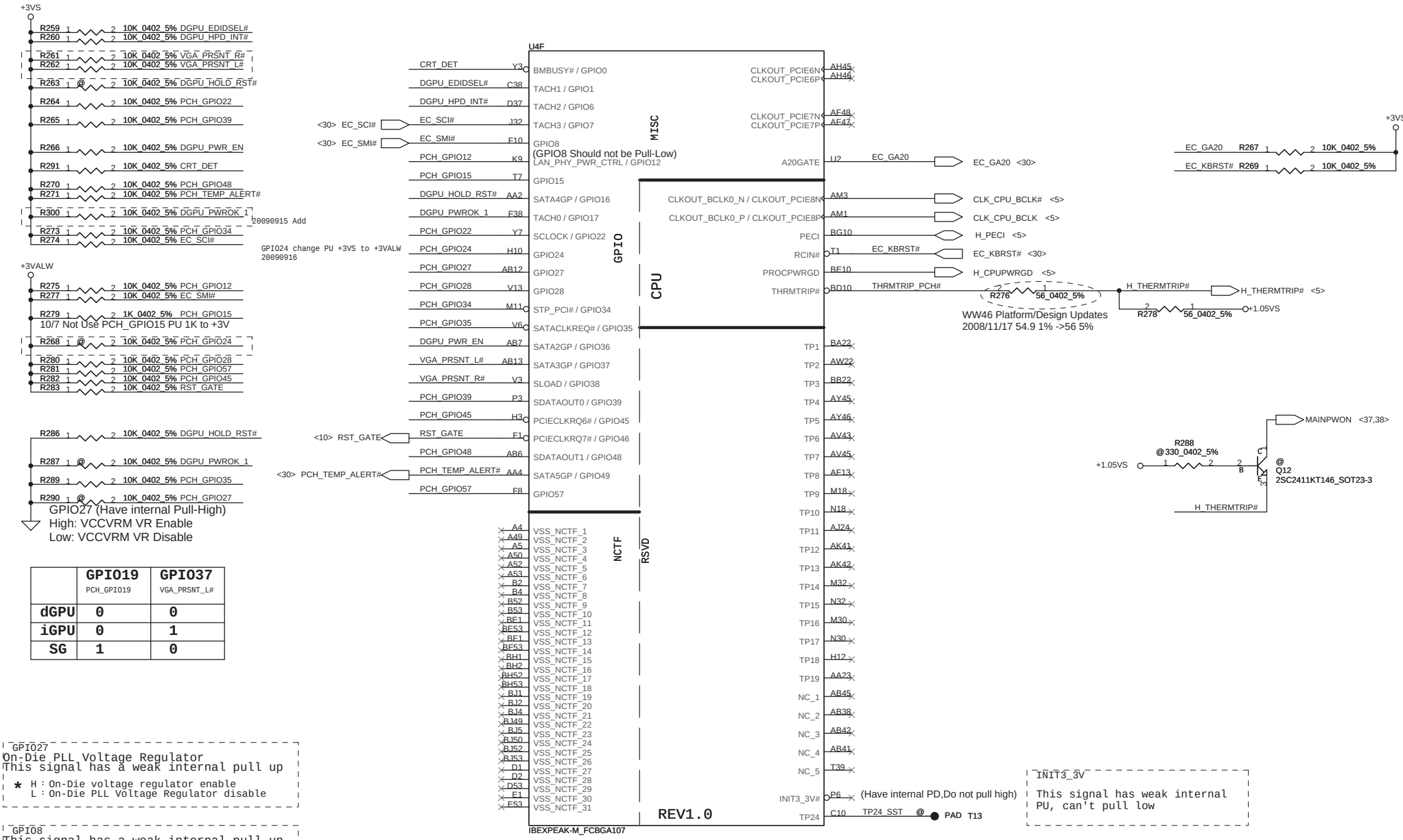

	GPIO19 PCH_GPIO19	GPIO37 VGA_PRSNT_L#
dGPU	0	0
iGPU	0	1
SG	1	0

GPIO27
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

GPIO8
This signal has a weak internal pull up
can't Pull low

GPIO15
L : Intel ME Crypto Transport Layer Security(TLS) chiper suite with no confidentiality *

H : Intel ME Crypto Transport Layer Security(TLS) chiper suite with confidentiality

it have weak internal PU 20K

INIT3_3V
This signal has weak internal PU, can't pull low

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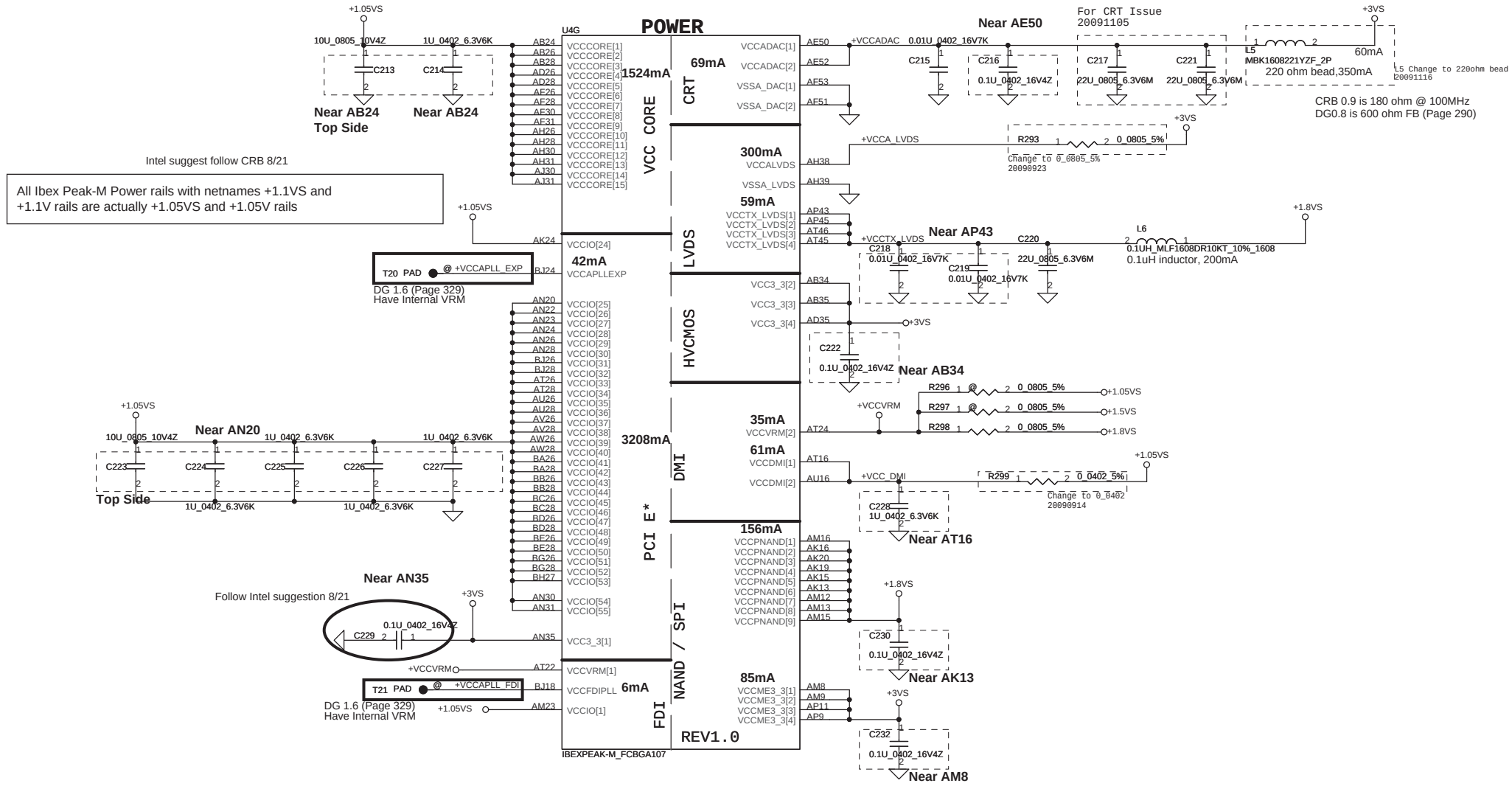

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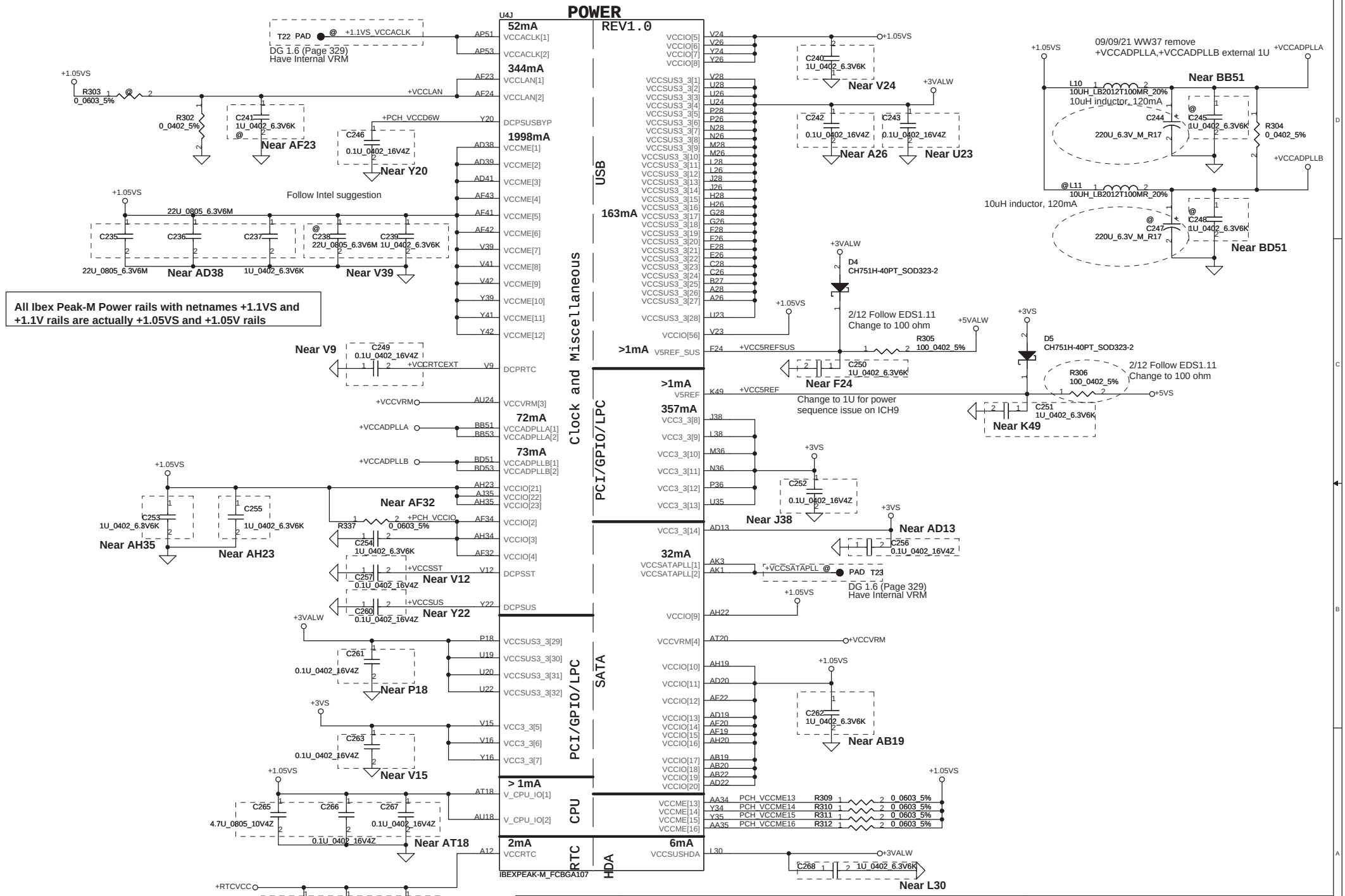

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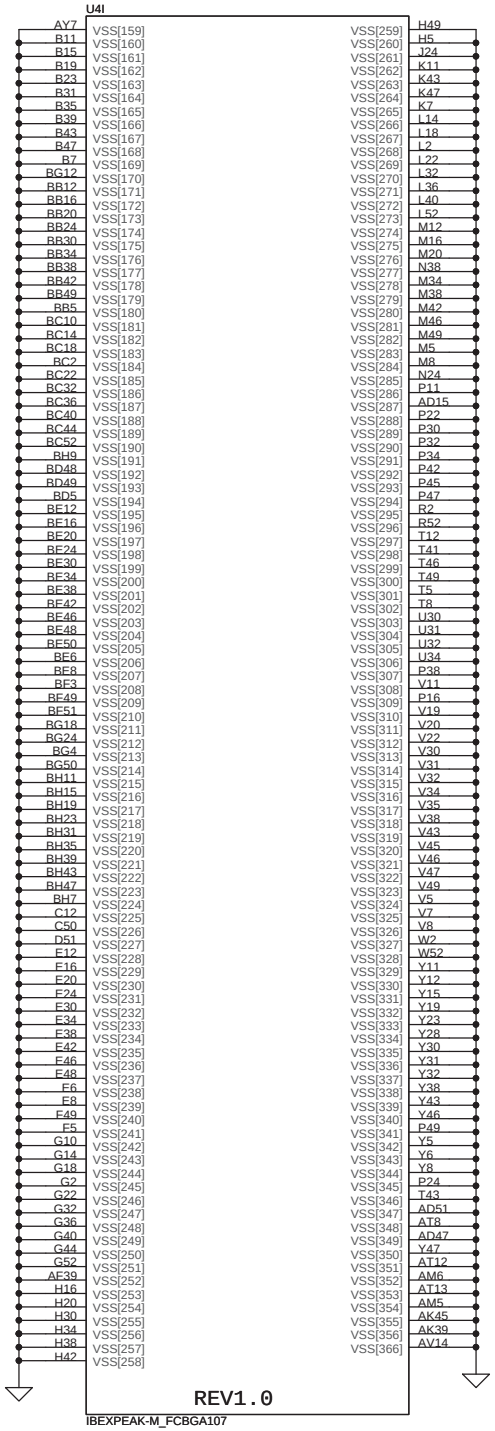

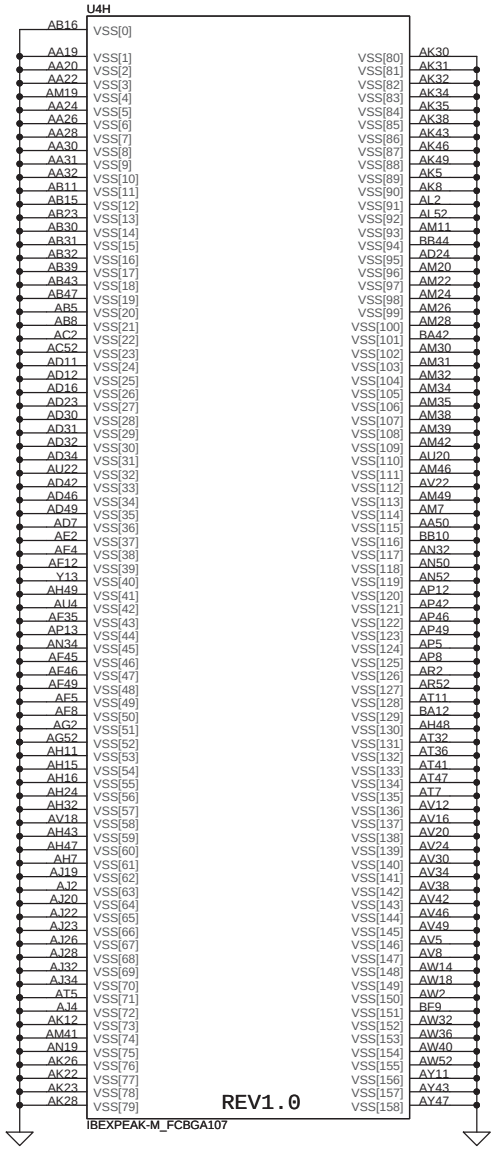

Del PCH XDP

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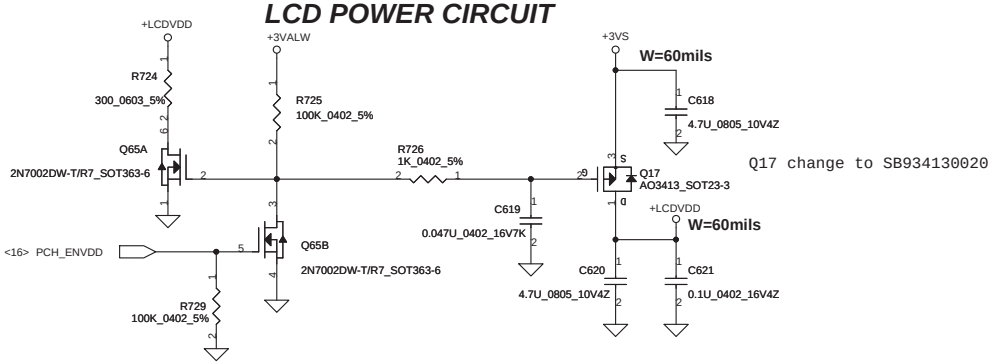
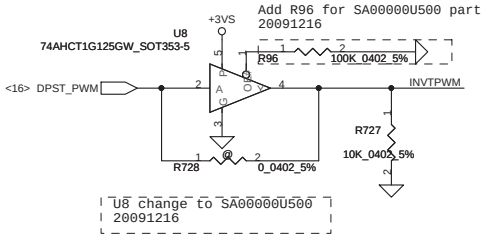
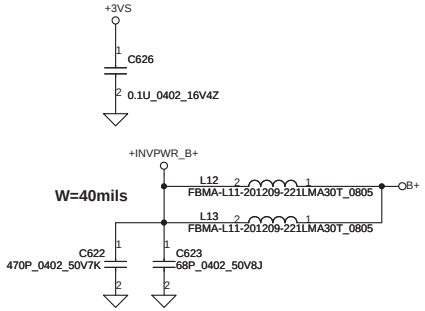
LCD POWER CIRCUIT

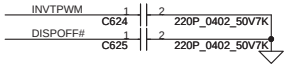


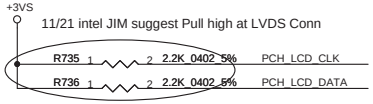
Q17 change to SB934130020

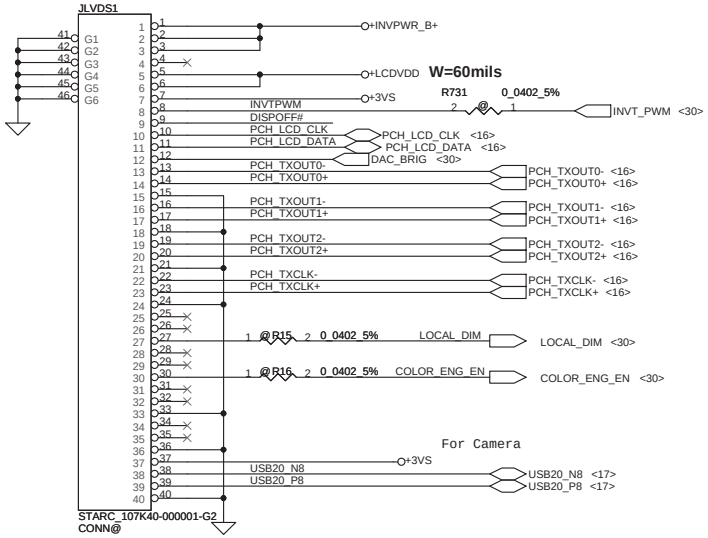


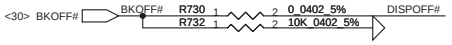
LED PANEL Conn.

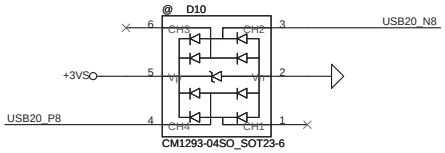












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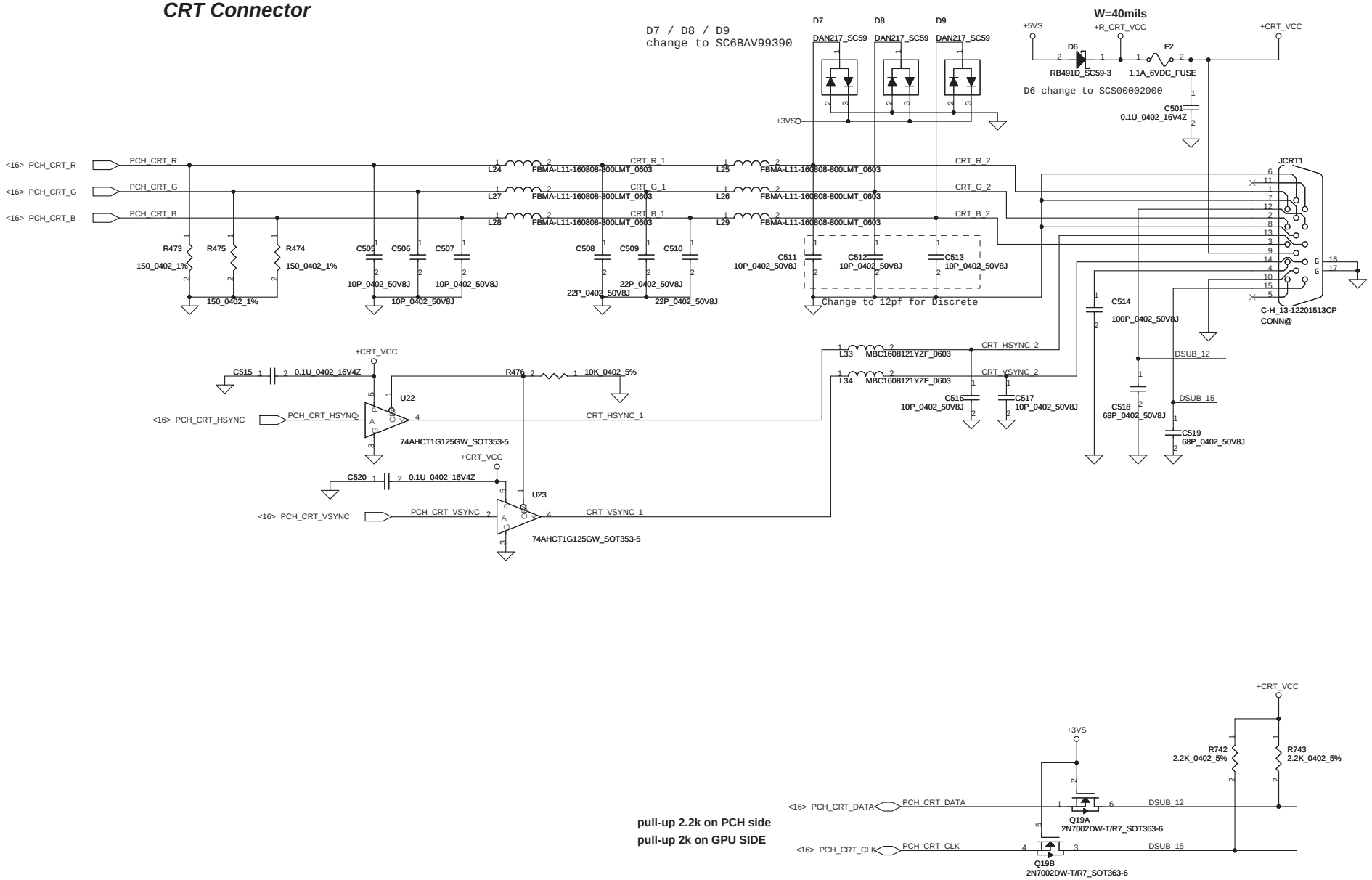
CRT Connector



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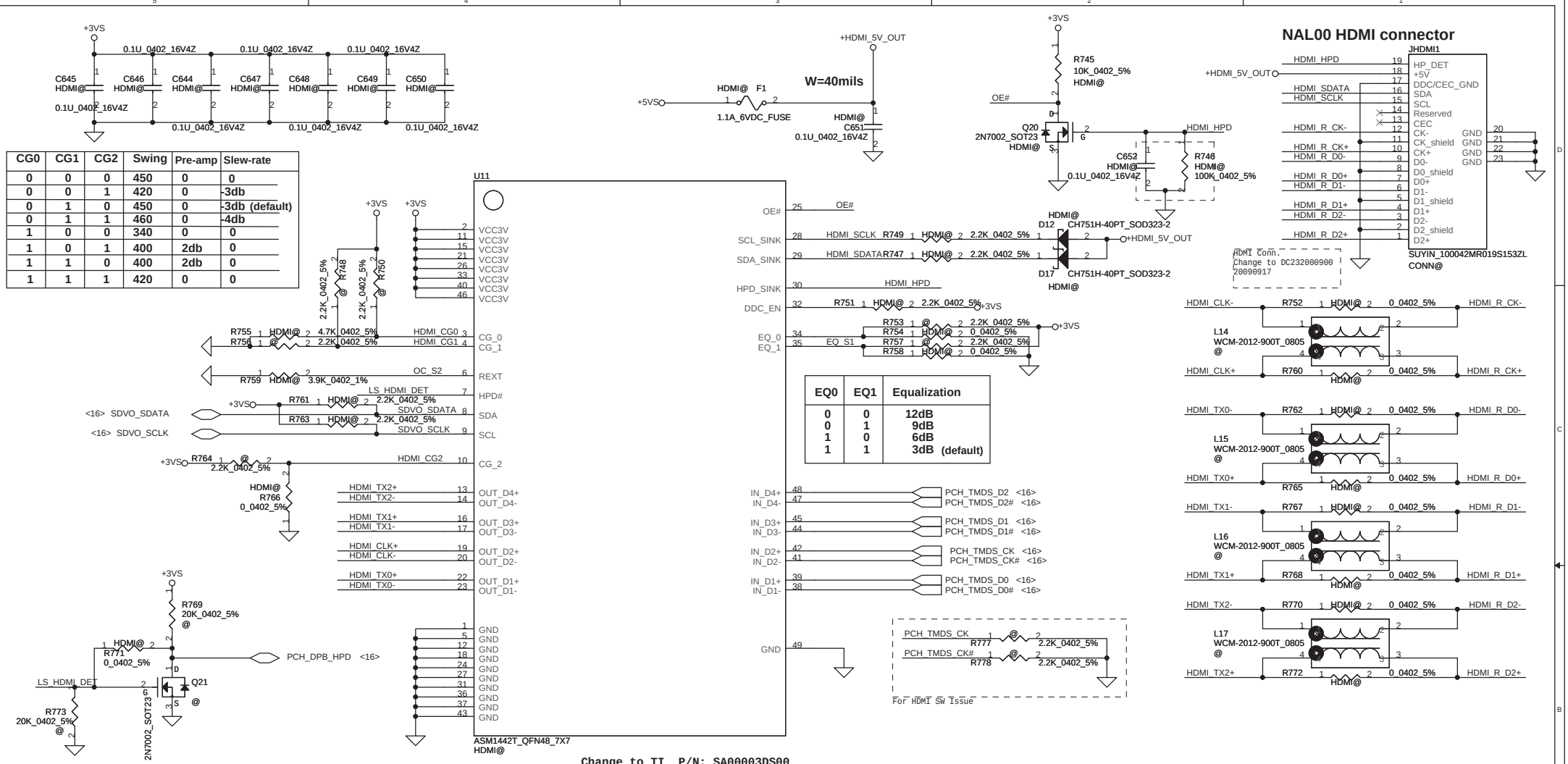

CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0

EQ0	EQ1	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB (default)

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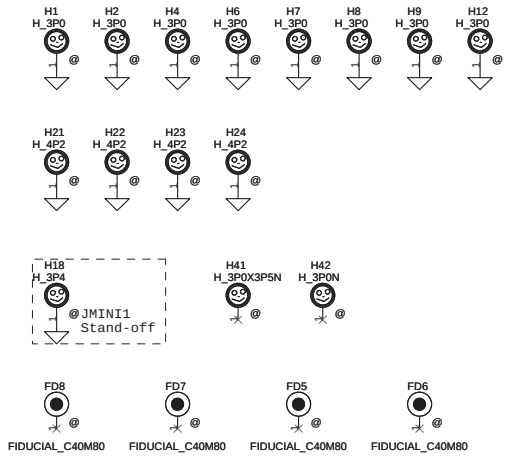
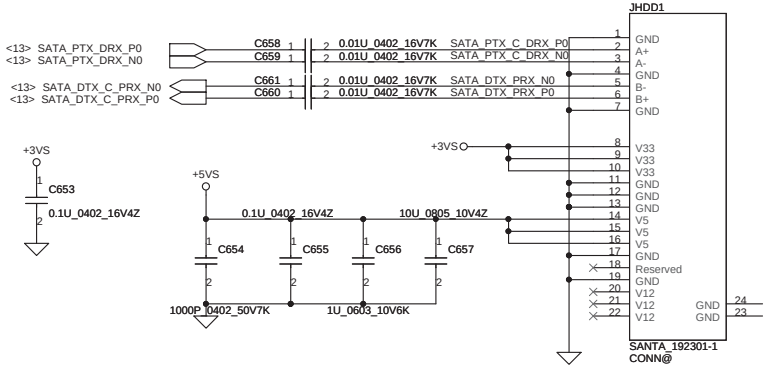


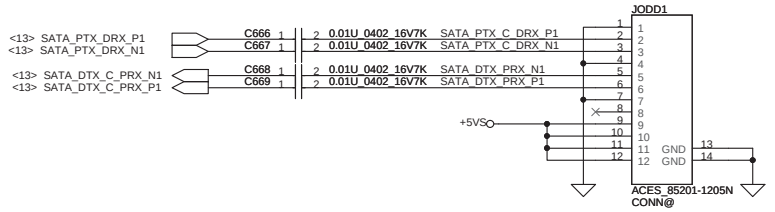
SATA HDD1 Conn.

CL 4.0 mm



20090915 Update to SANTA

SATA ODD FFC Conn.



Change to 12P conn. for FFC
20100413

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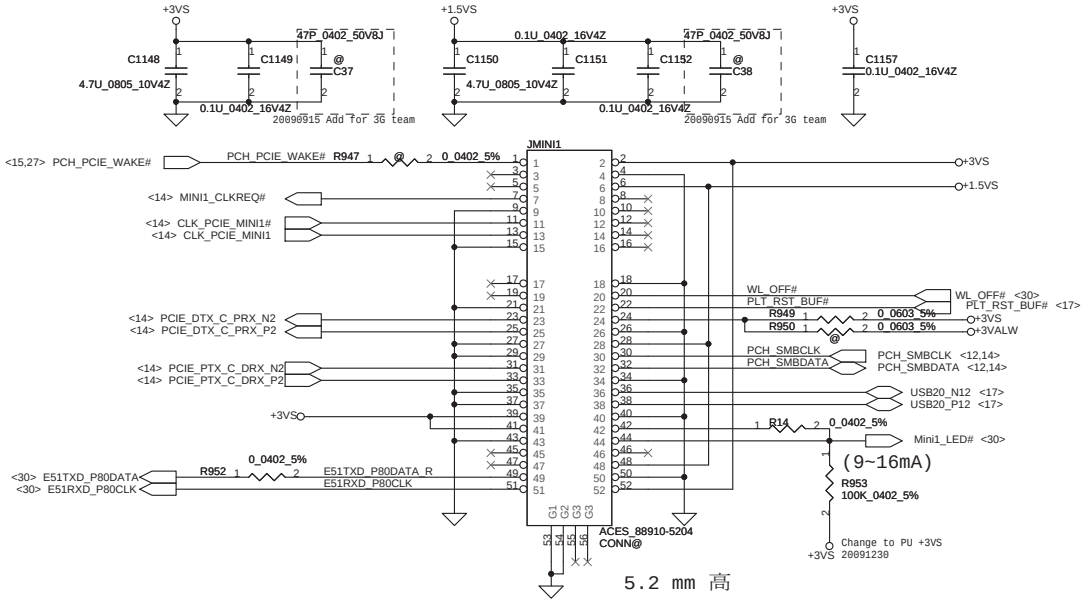
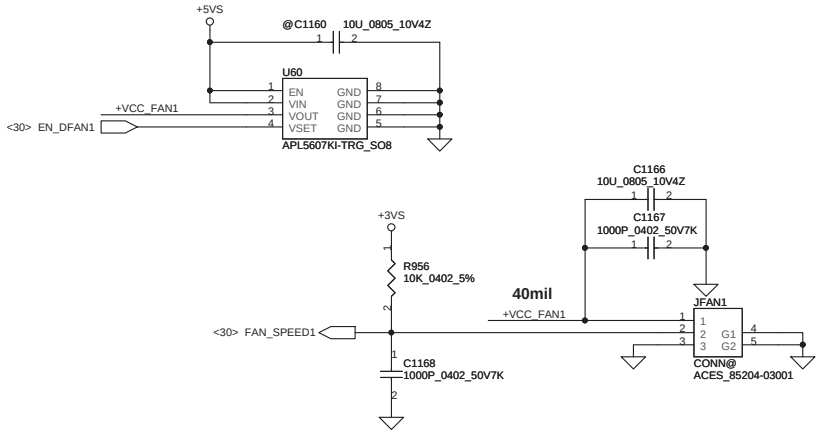
For Wireless LAN



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Del 3G / GPS Module Connect

FAN1 Conn



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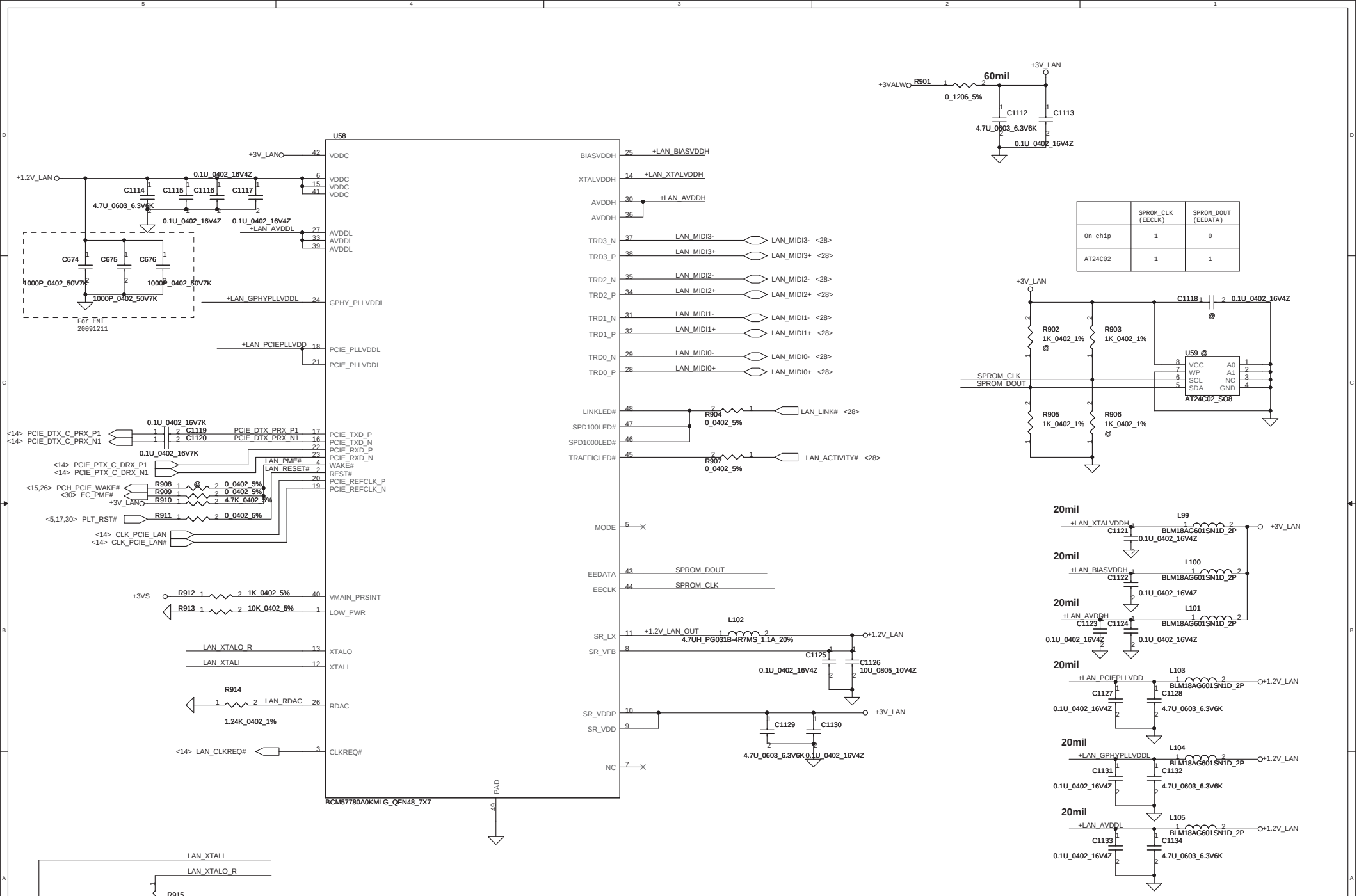

	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

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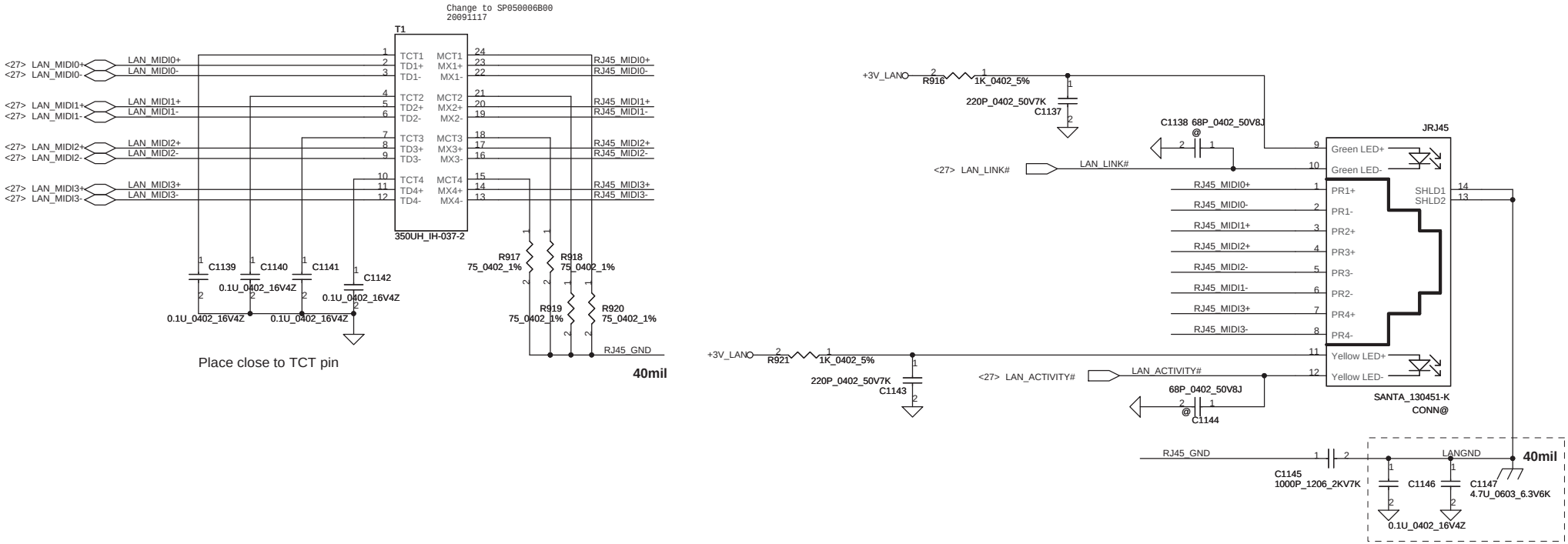
LAN Connector



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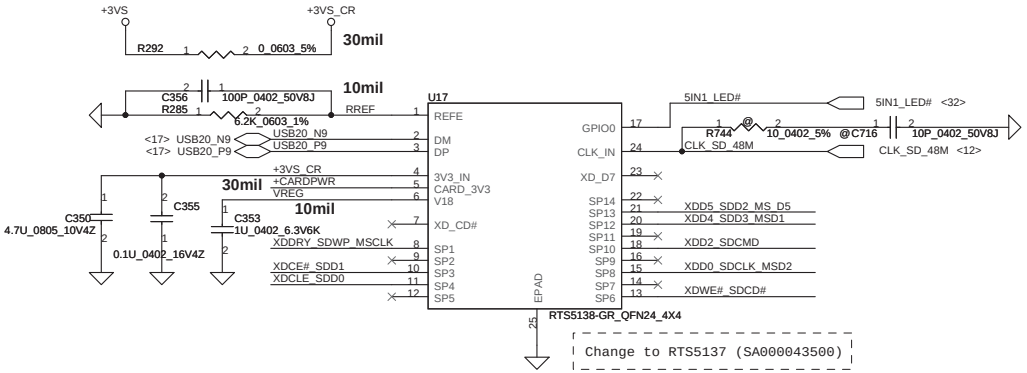
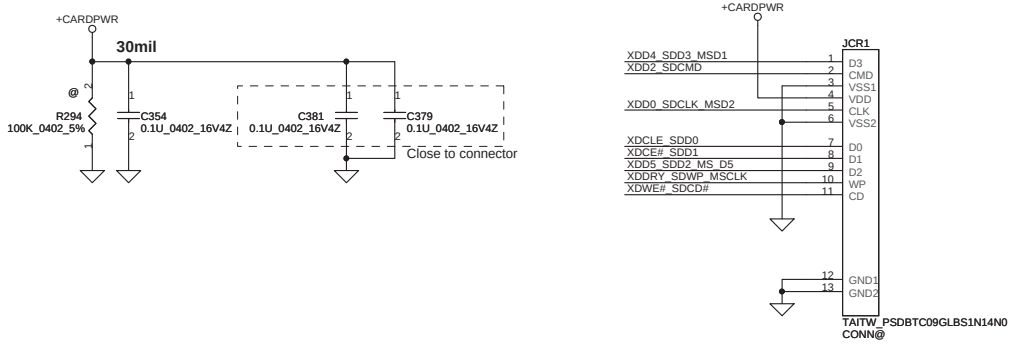
Card Reader RTS5138 / RTS5137
(only SD+MMC function)

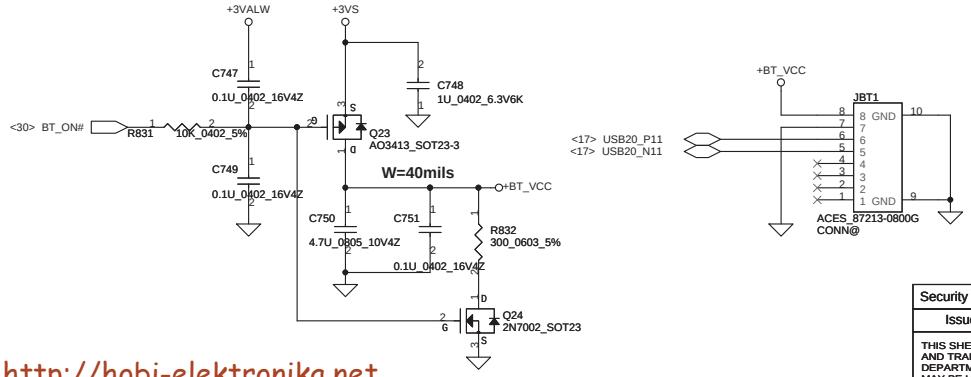


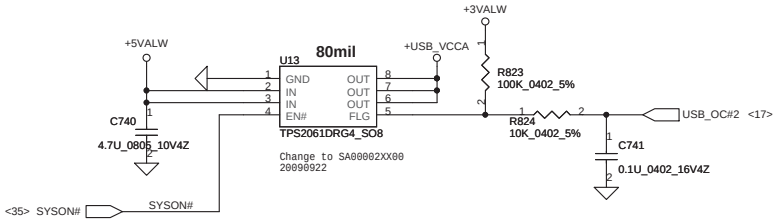
Card Reader Connector

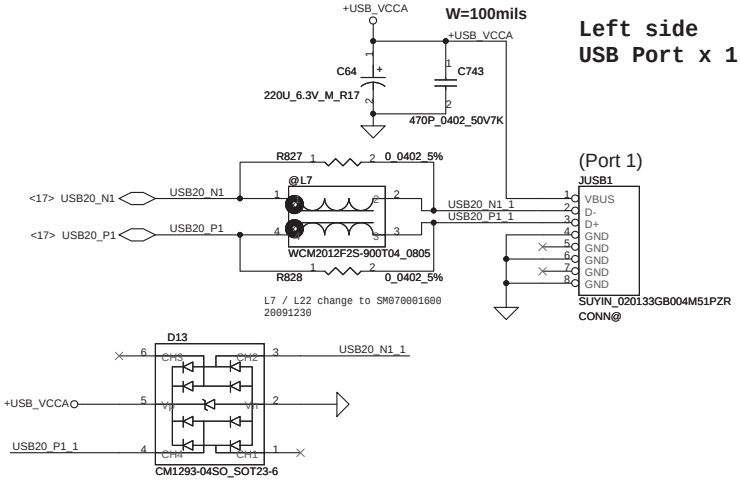


Bluetooth Conn.

Q23 change to SB934130020

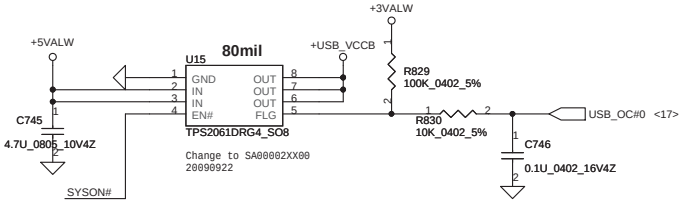






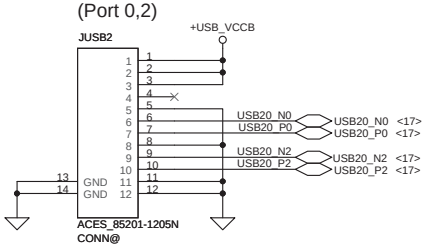
Left side
USB Port x 1

(Port 1)



USB/B Conn.

(Port 0,2)



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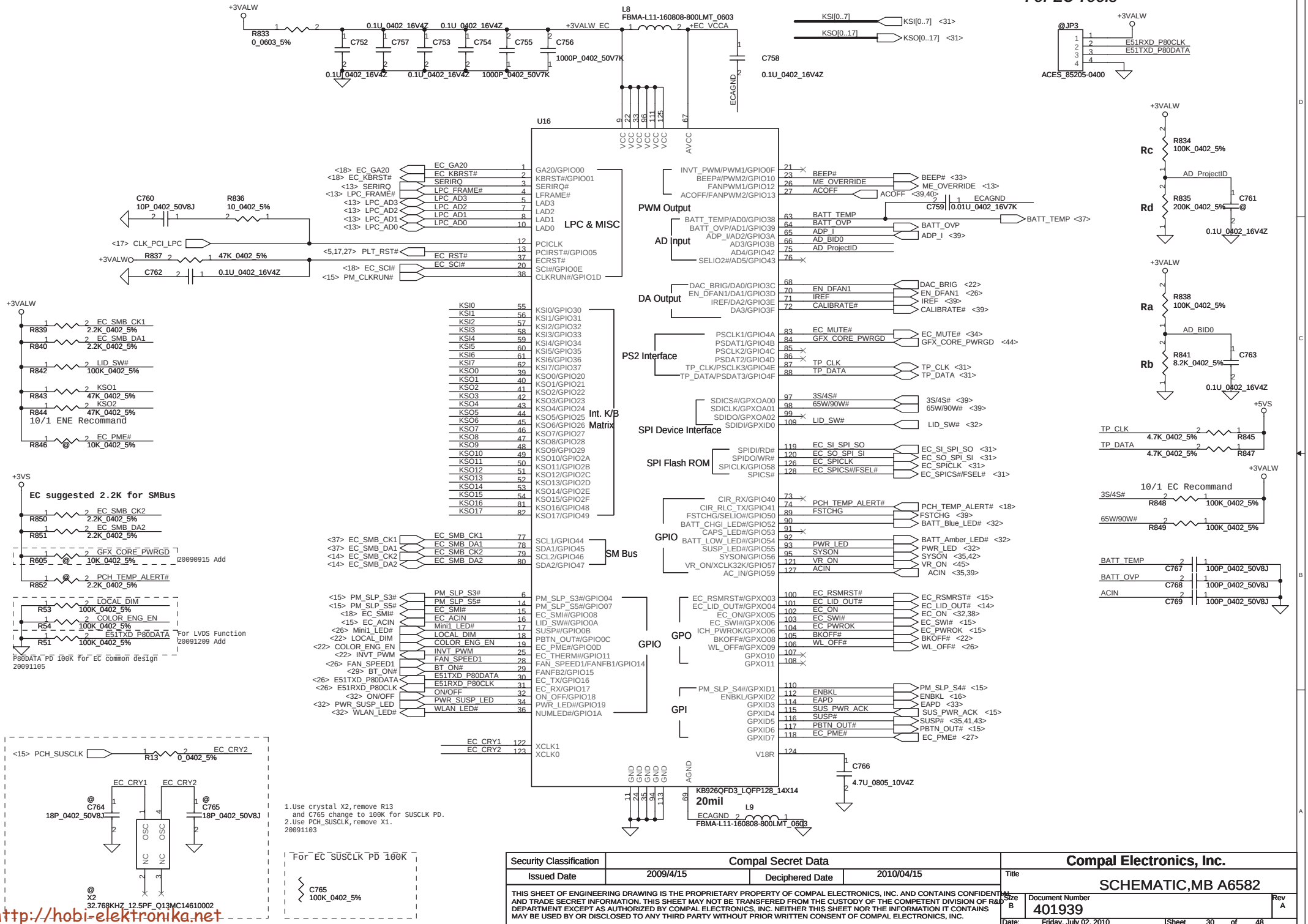

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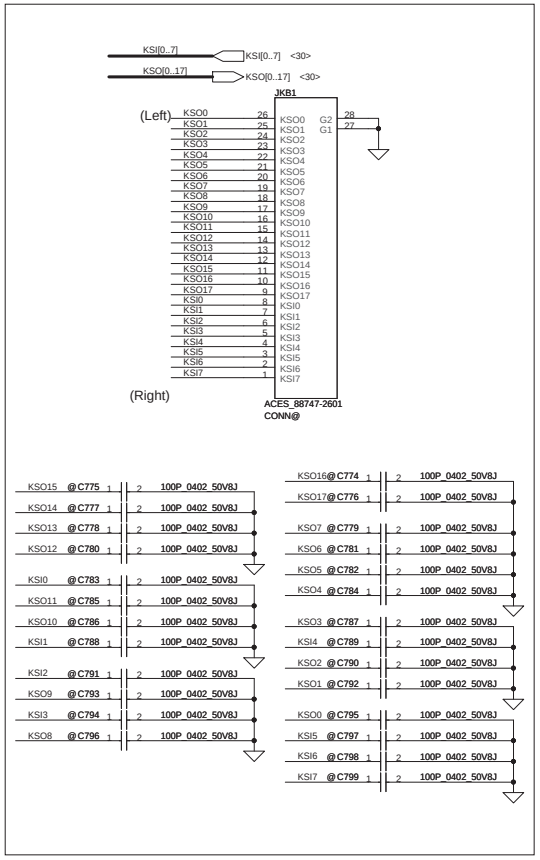

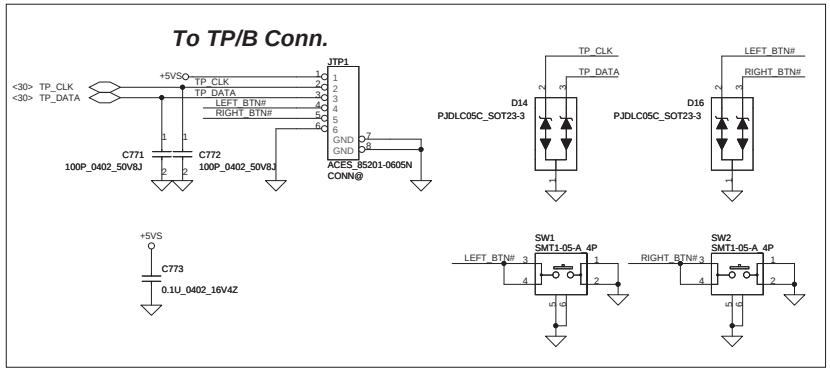

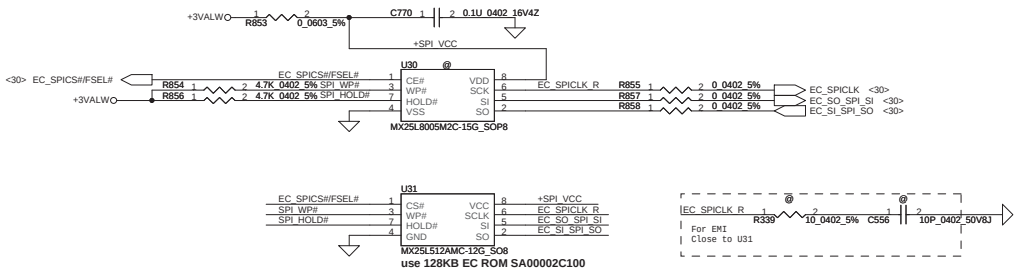

ENE suggestion SPI Frequency over 66MHz
SST: 50MHz
MXIC: 70MHz
ST: 40MHz

To BTN/B Conn.

	KSO0	KSO3
KSI1	WL_BTN#	Program_BTN#
KSI2	T/P lock_BTN#	
KSI3	Back up_BTN#	Volum up_BTN# Volum down_BTN#
KSI4	BT_BTN#	
KSI5	Power save_BTN#	

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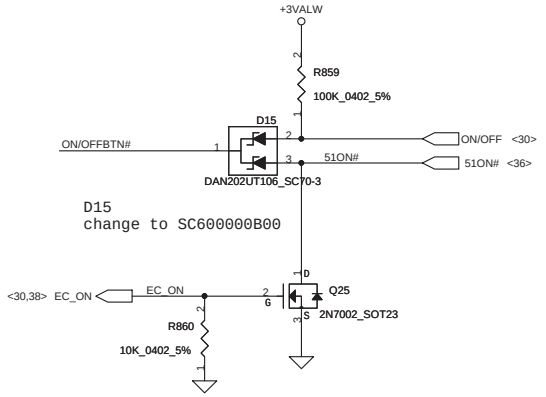
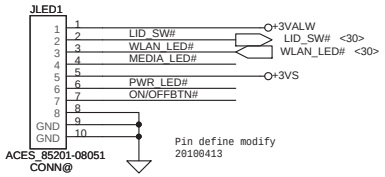
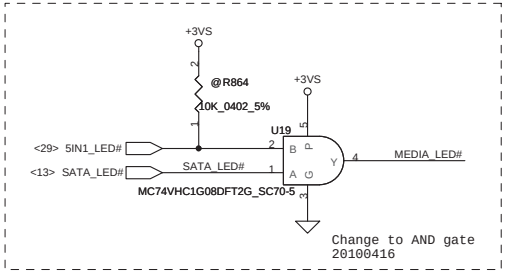
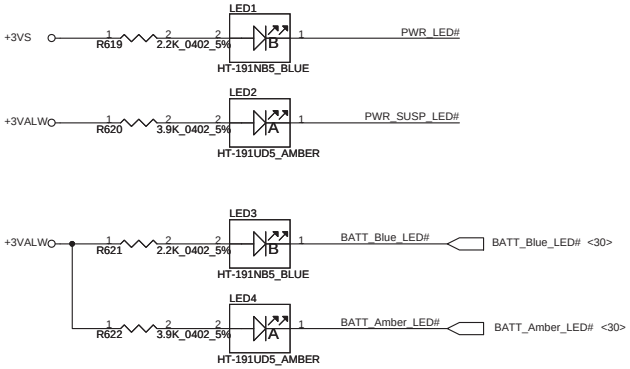
Power Button

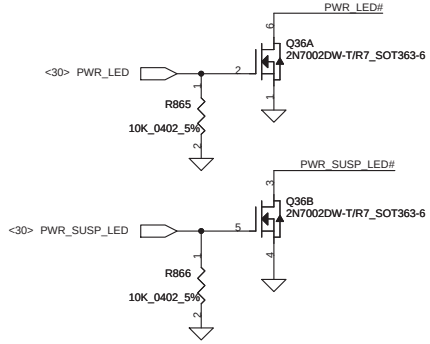


LED/B LEFT









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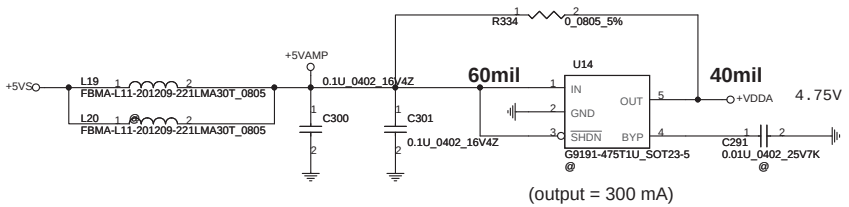
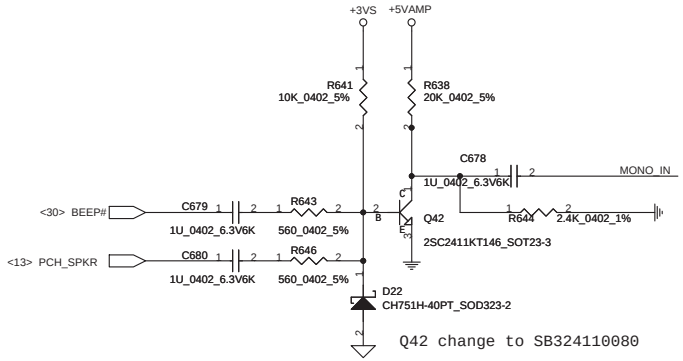
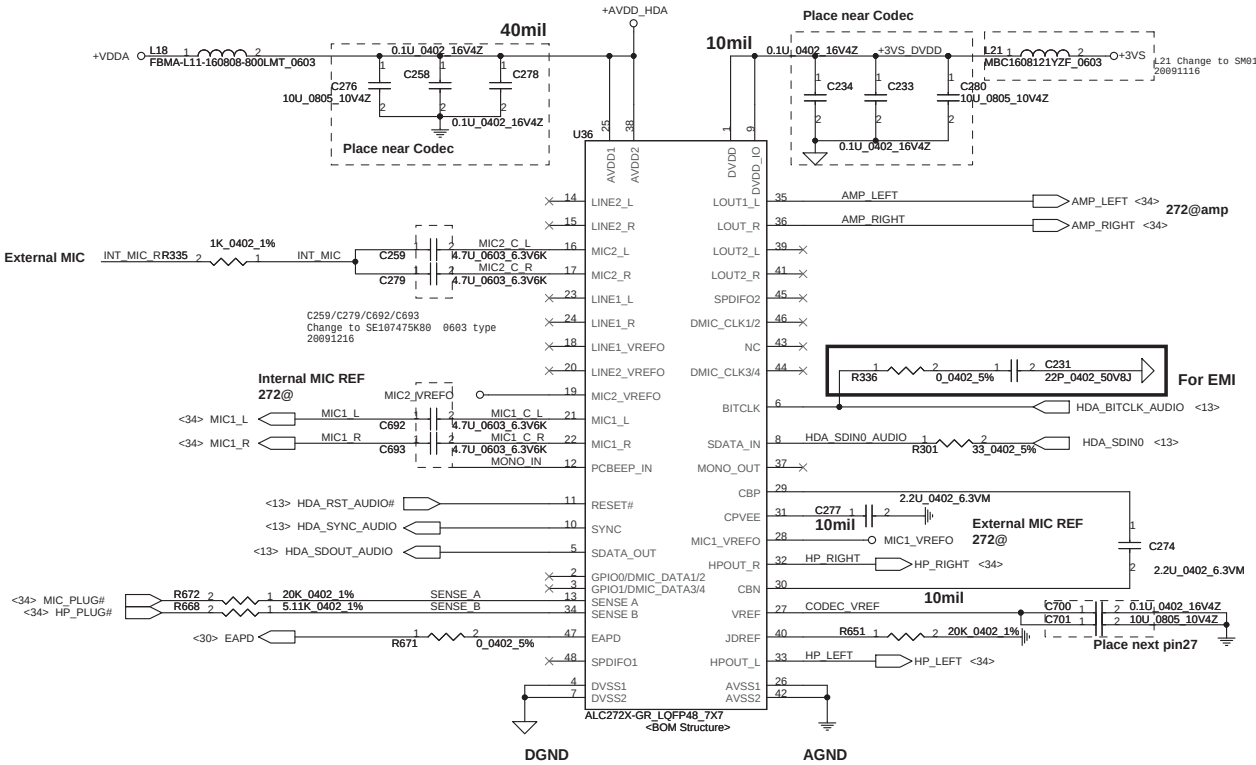
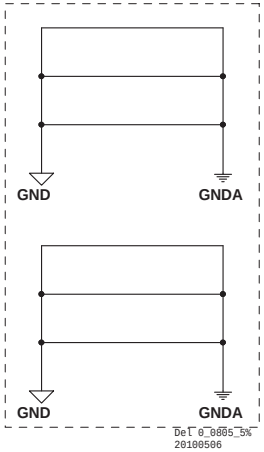
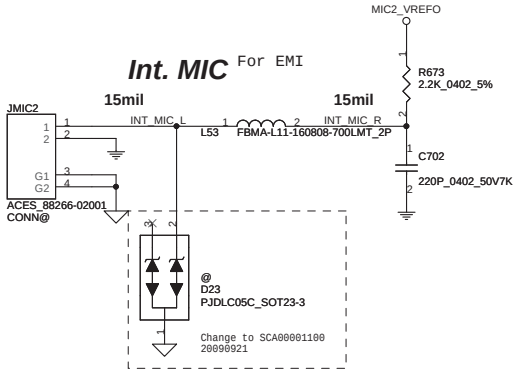




HD Audio Codec







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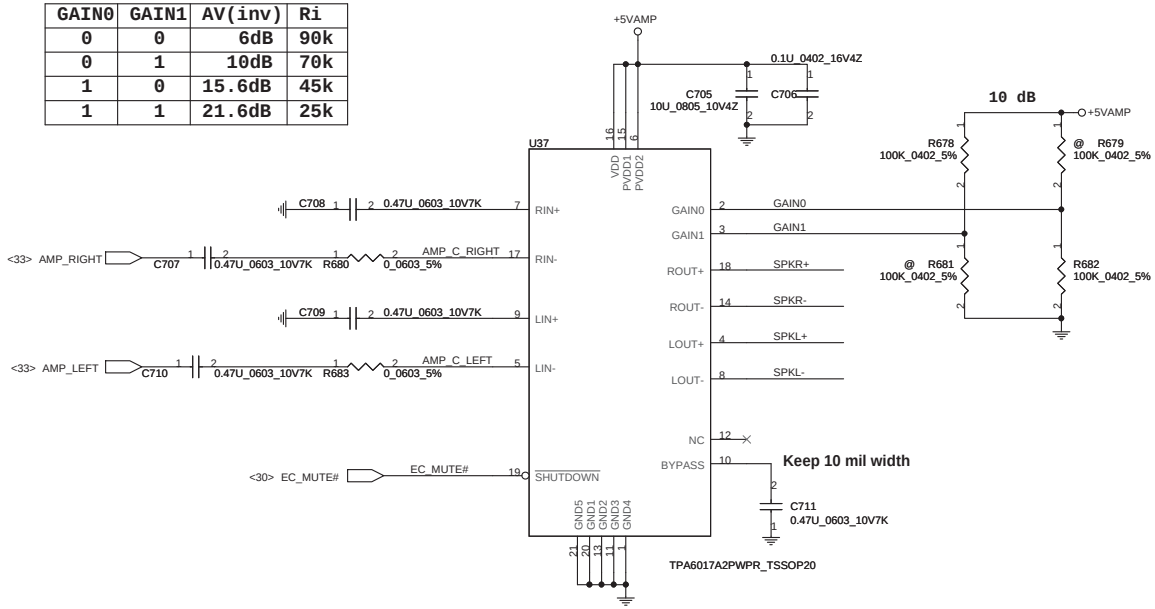
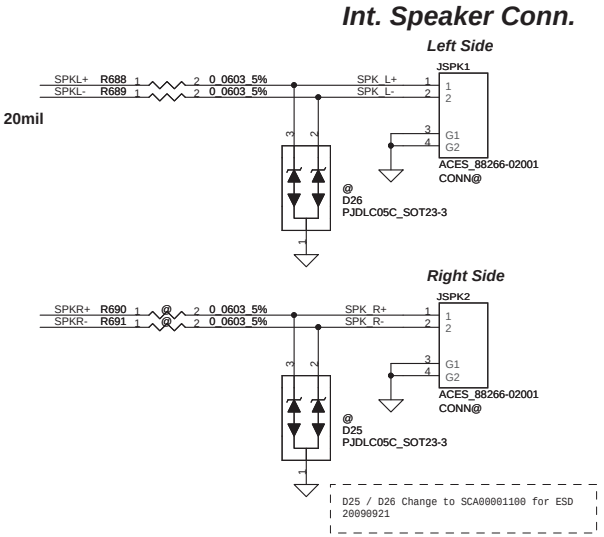
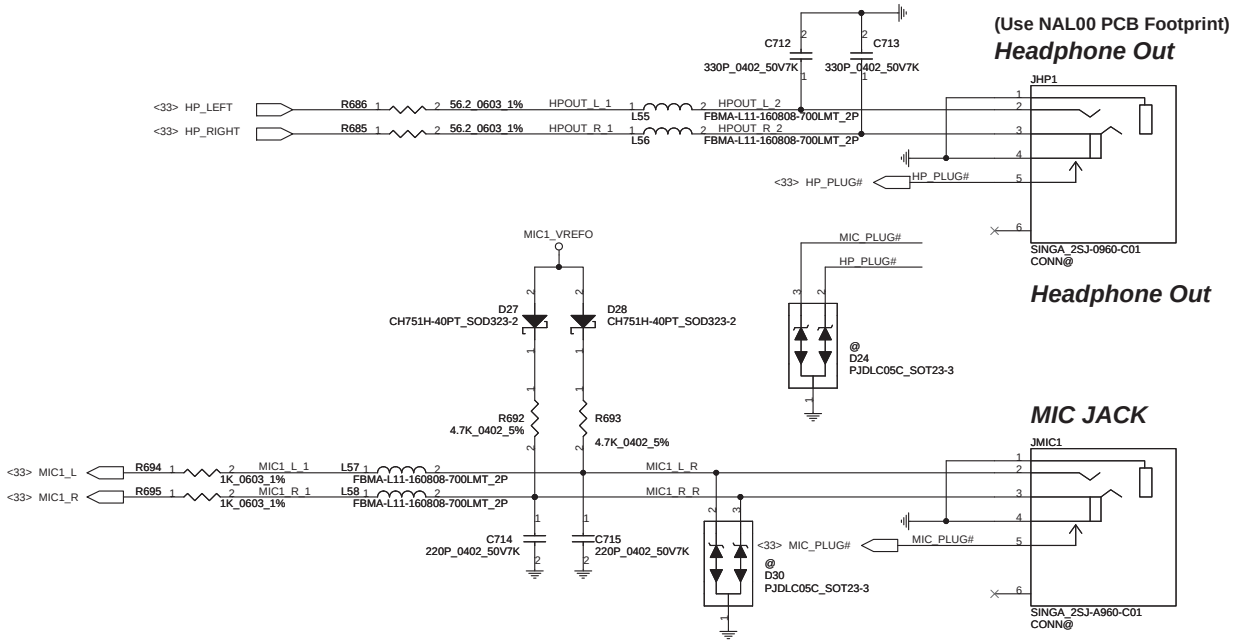
GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k







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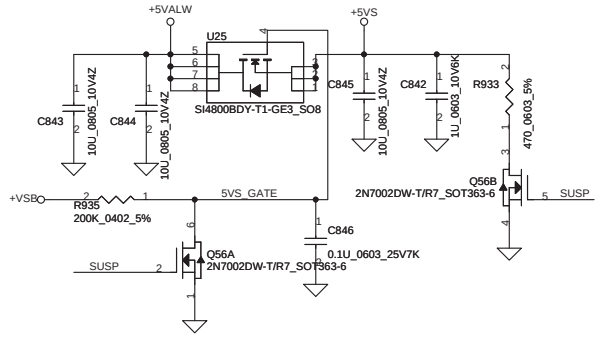
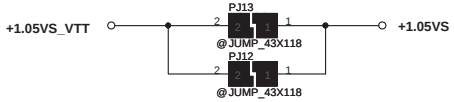
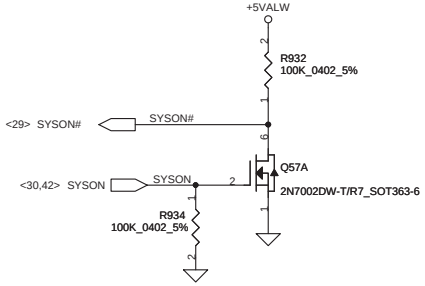
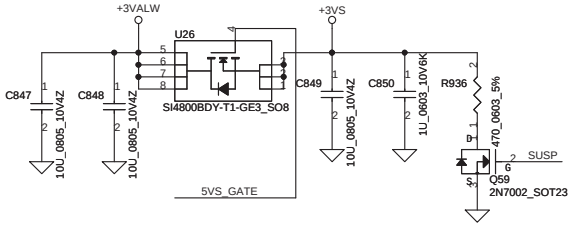
+5VALW TO +5VS

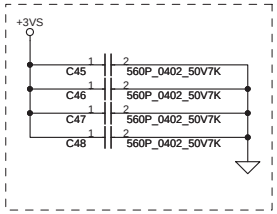




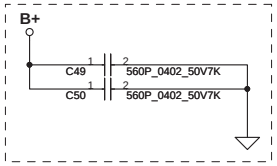


+3VALW TO +3VS

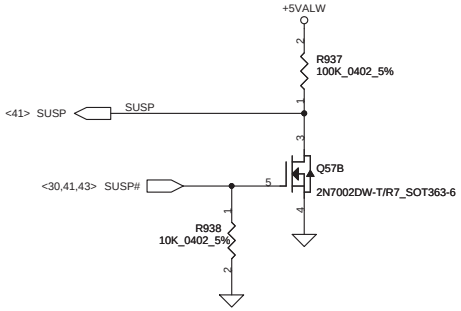




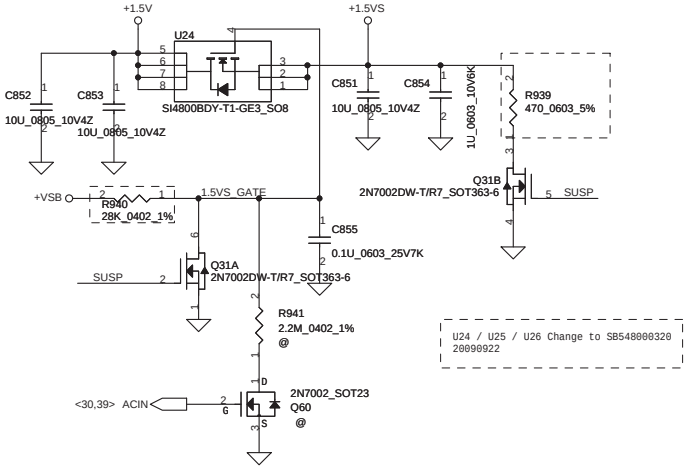
For LAM Common mode noise
200911102330



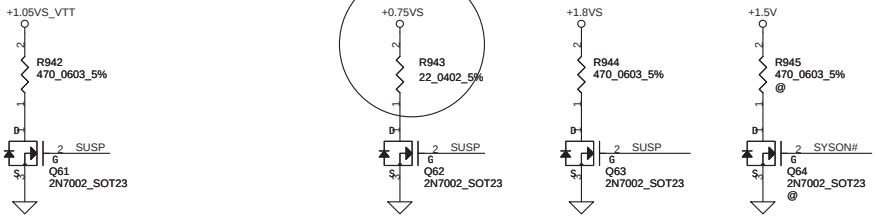
For EC B+
20100507



+1.5V to +1.5VS



U24 / U25 / U26 Change to SB548000320
20090922



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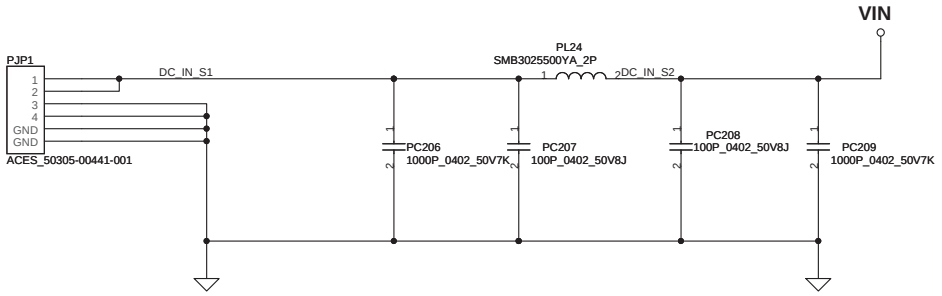

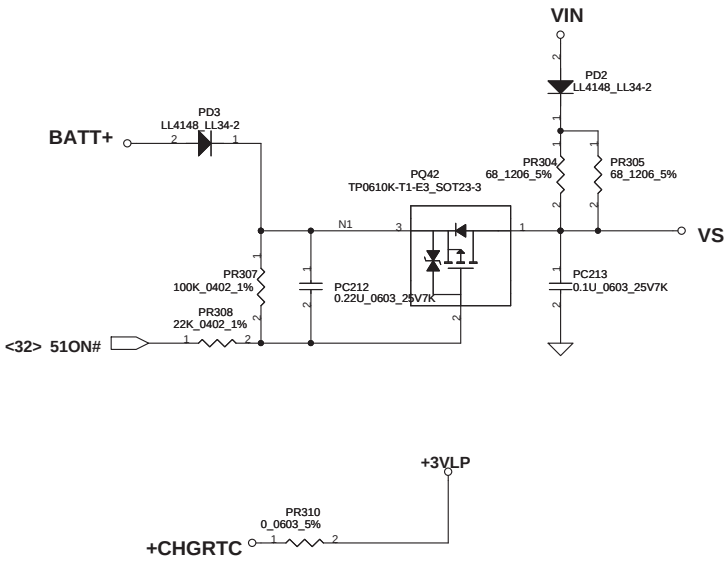

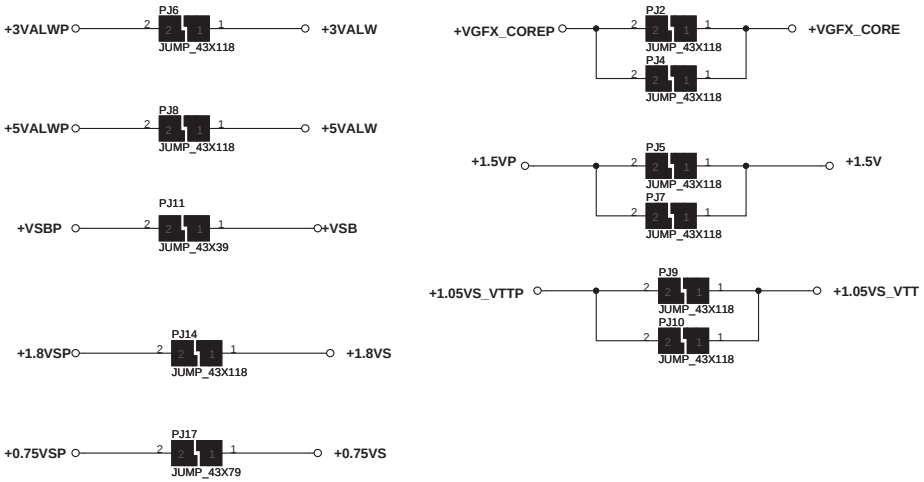

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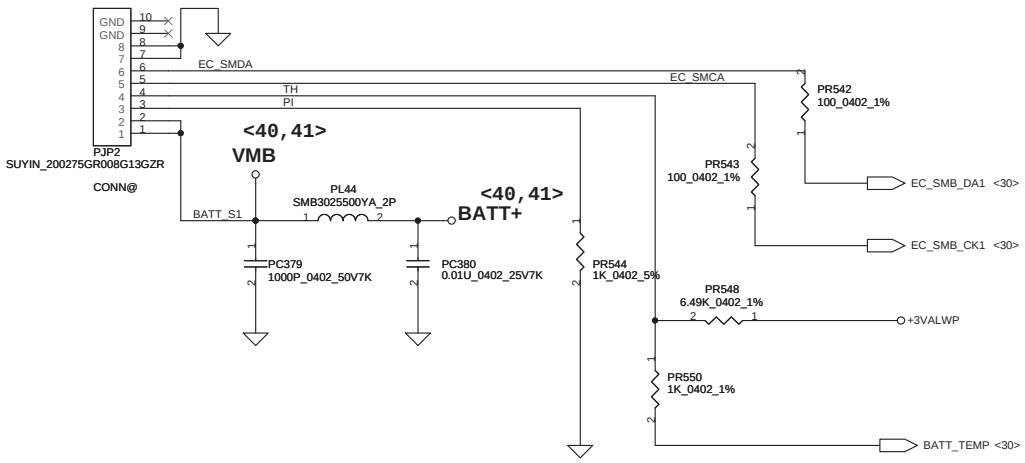
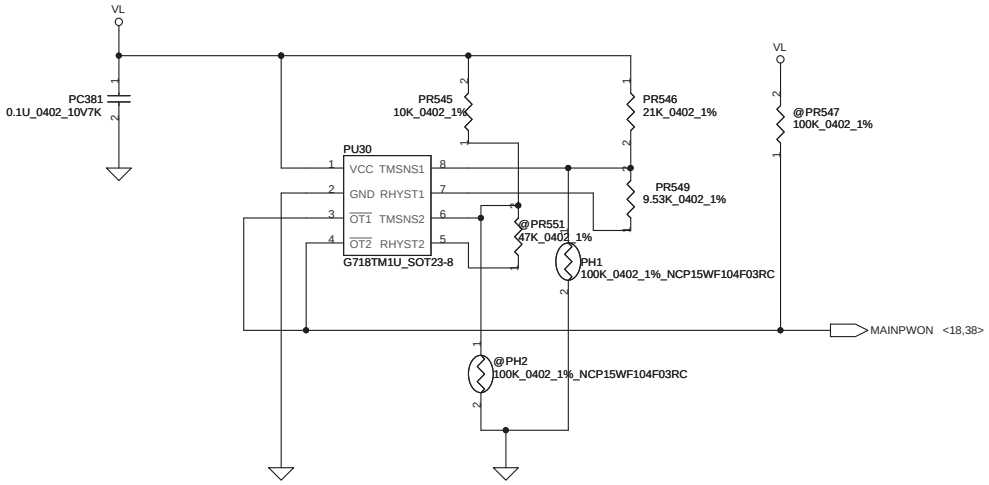
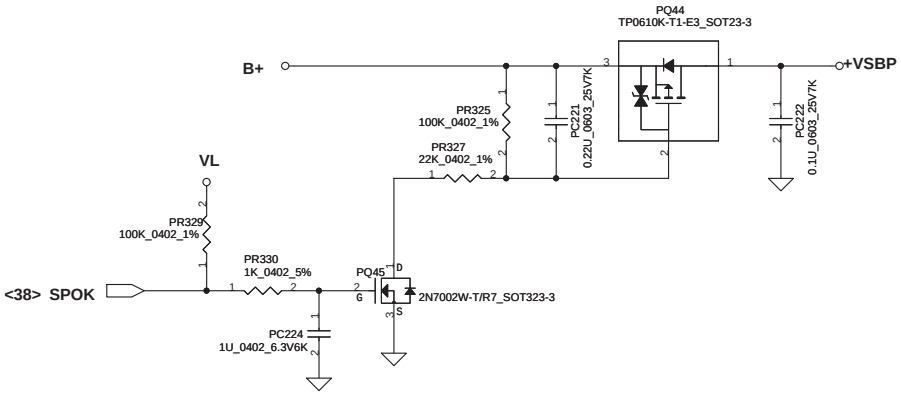


PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C





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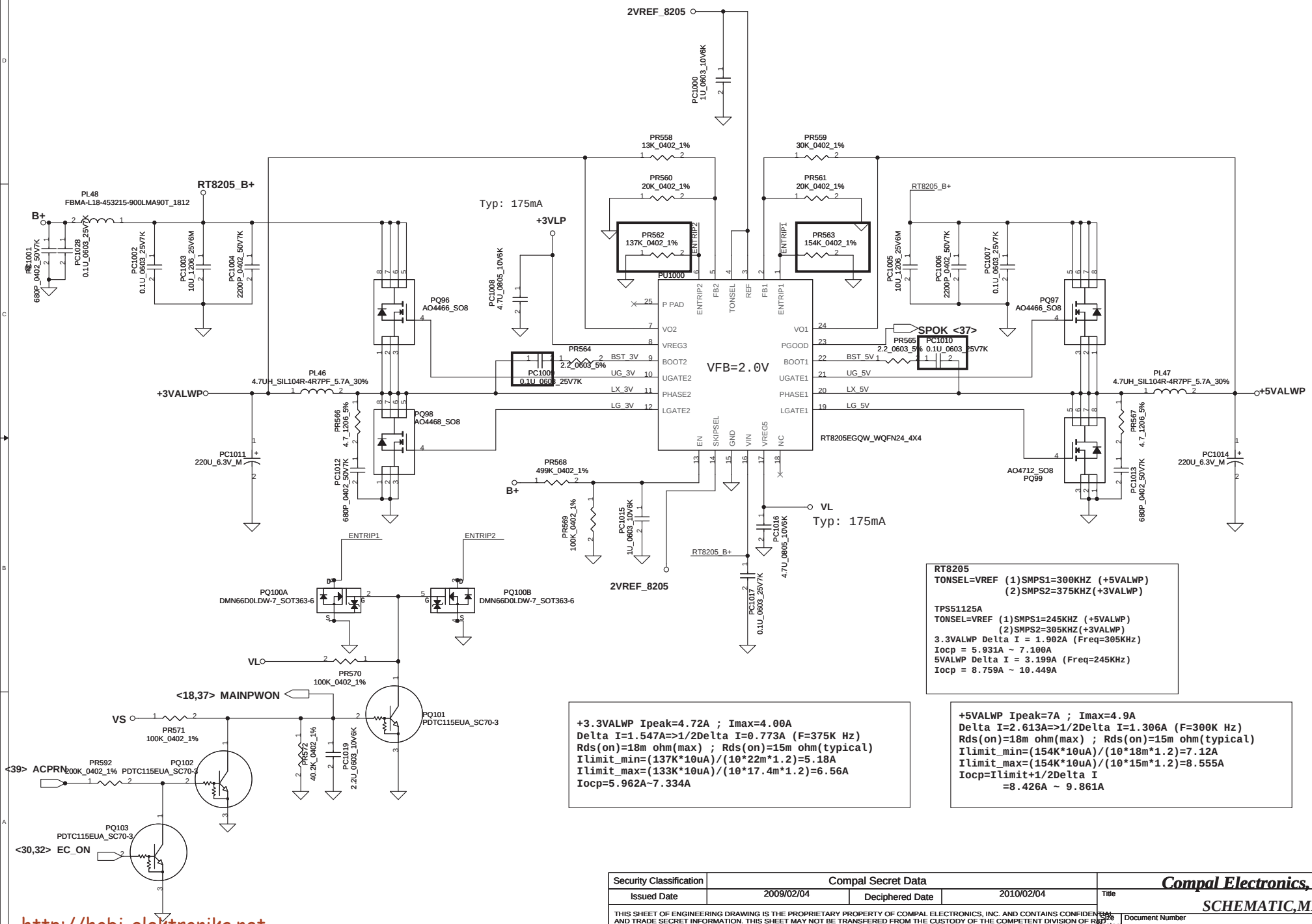
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



RT8205
TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)
(2)SMPS2=375KHZ(+3VALWP)

TPS51125A
TONSEL=VREF (1)SMPS1=245KHZ (+5VALWP)
(2)SMPS2=305KHZ(+3VALWP)
3.3VALWP Delta I = 1.902A (Freq=305KHz)
Iocp = 5.931A ~ 7.100A
5VALWP Delta I = 3.199A (Freq=245KHz)
Iocp = 8.759A ~ 10.449A

+3.3VALWP Ipeak=4.72A ; Imax=4.00A
Delta I=1.547A=>1/2Delta I=0.773A (F=375K Hz)
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Ilimit_min=(137K*10uA)/(10*22m*1.2)=5.18A
Ilimit_max=(133K*10uA)/(10*17.4m*1.2)=6.56A
Iocp=5.962A~7.334A

+5VALWP Ipeak=7A ; Imax=4.9A
Delta I=2.613A=>1/2Delta I=1.306A (F=300K Hz)
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Ilimit_min=(154K*10uA)/(10*18m*1.2)=7.12A
Ilimit_max=(154K*10uA)/(10*15m*1.2)=8.555A
Iocp=Ilimit+1/2Delta I
=8.426A ~ 9.861A

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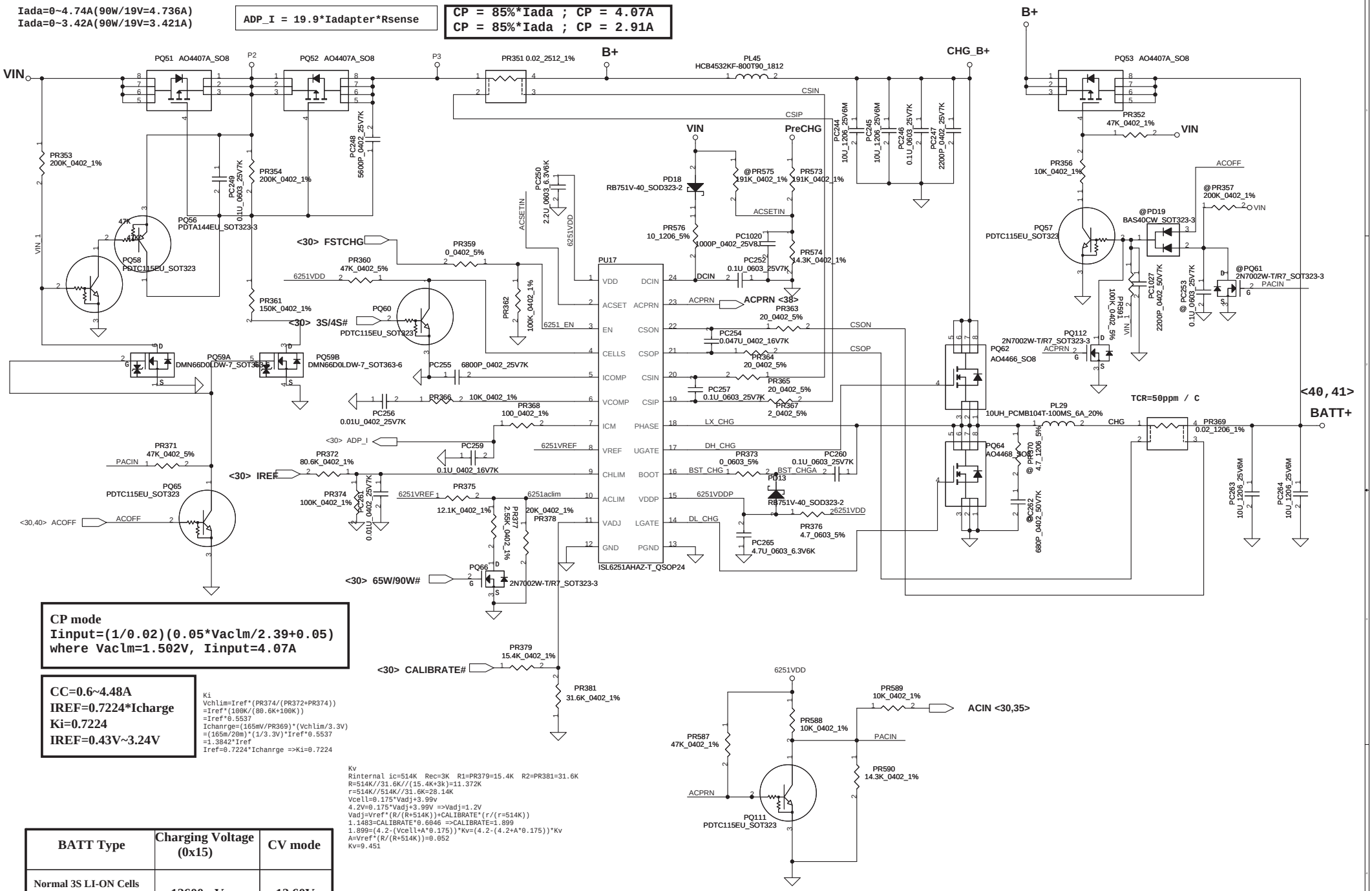
Iada=0~4.74A(90W/19V=4.736A)
Iada=0~3.42A(90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

CC=0.6~4.48A
IREF=0.7224*Icharge
Ki=0.7224
IREF=0.43V~3.24V

```
Ki
Vchlim=Iref*(PR374/(PR372+PR374))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichanrge=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichanrge =>Ki=0.7224
```

```
Kv
Rinternal ic=514K  Rec=3K  R1=PR379=15.4K  R2=PR381=31.6K
R=514K//31.6K//(15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451
```

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

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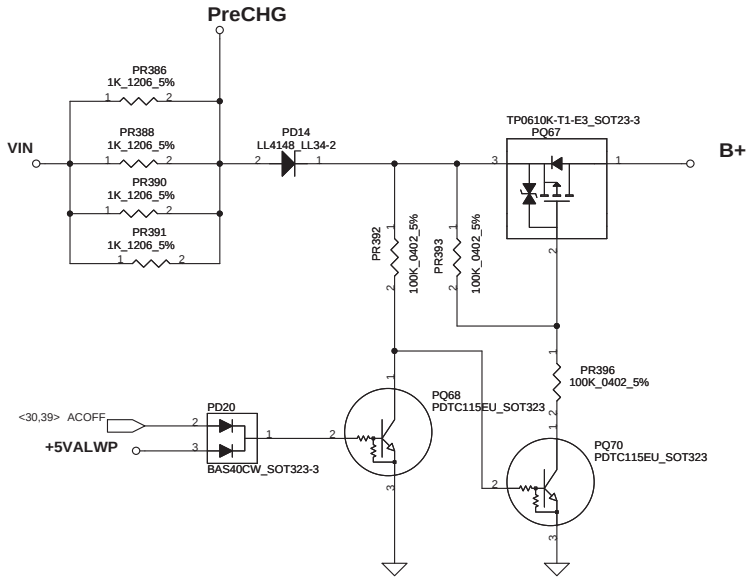

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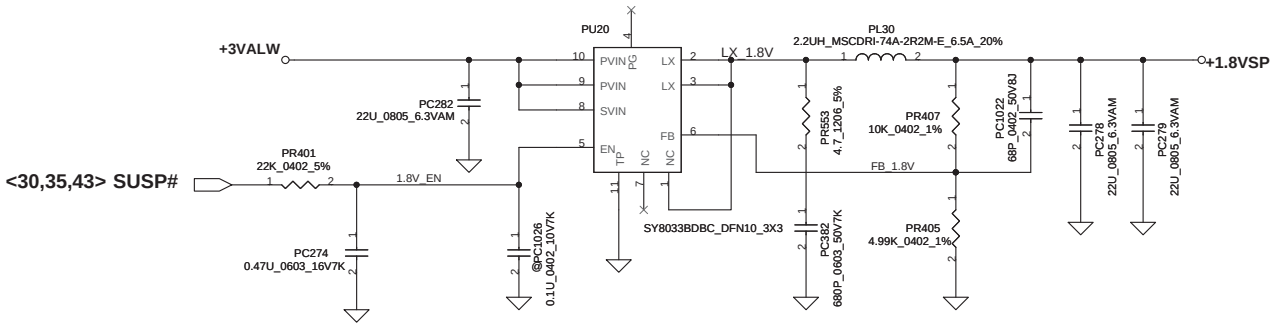
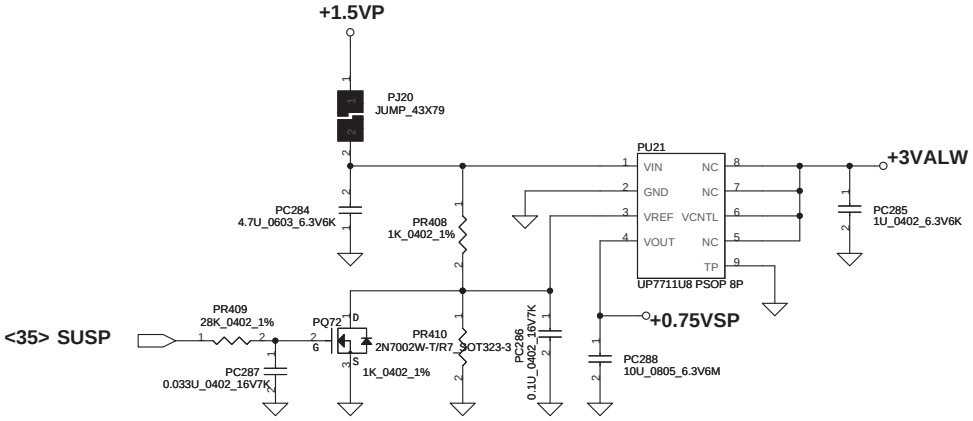
FB=0.6V
Note:Iload(max)=3.5A





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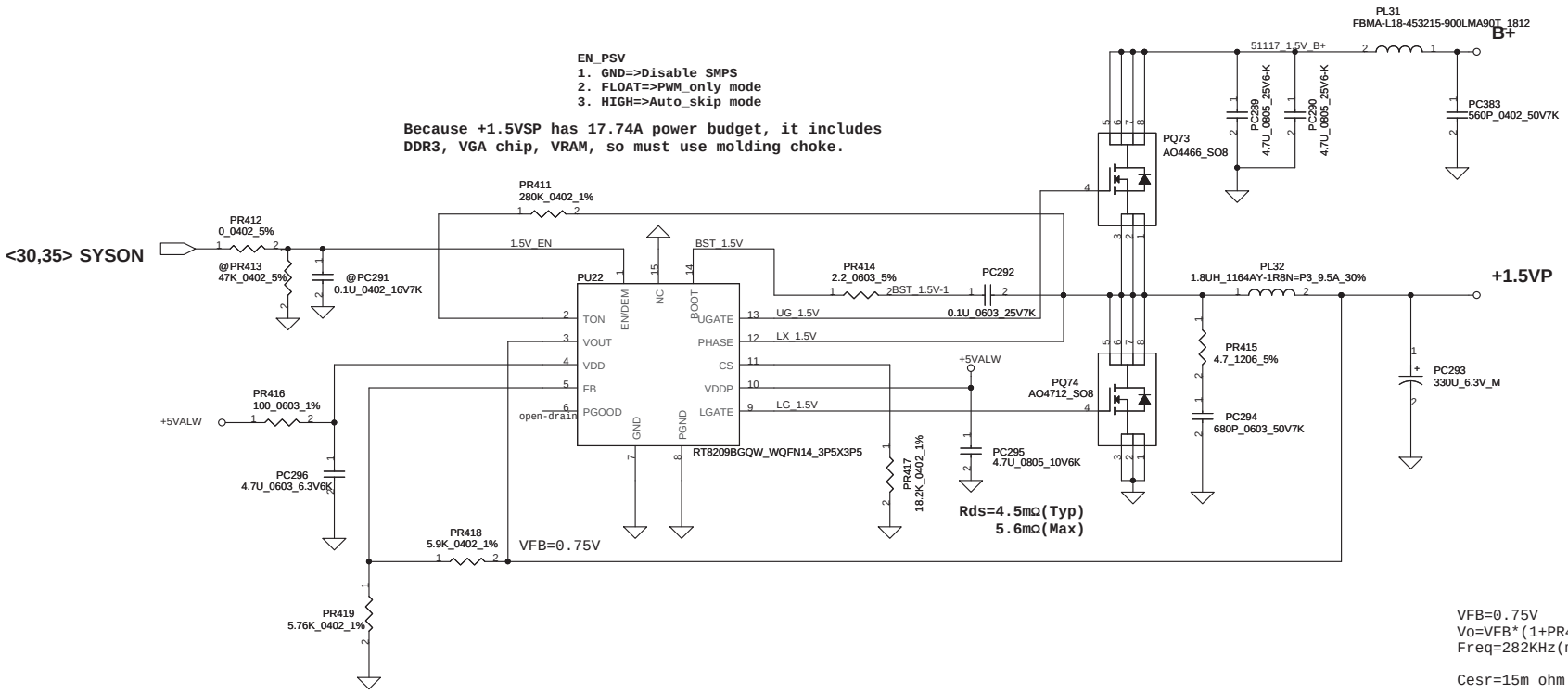

VFB=0.75V
Vo=VFB*(1+PR418/PR419)=1.52V
Freq=282KHz(min) , 300KHz(typ)

Cesr=15m ohm

Iocp=9.94A~13A

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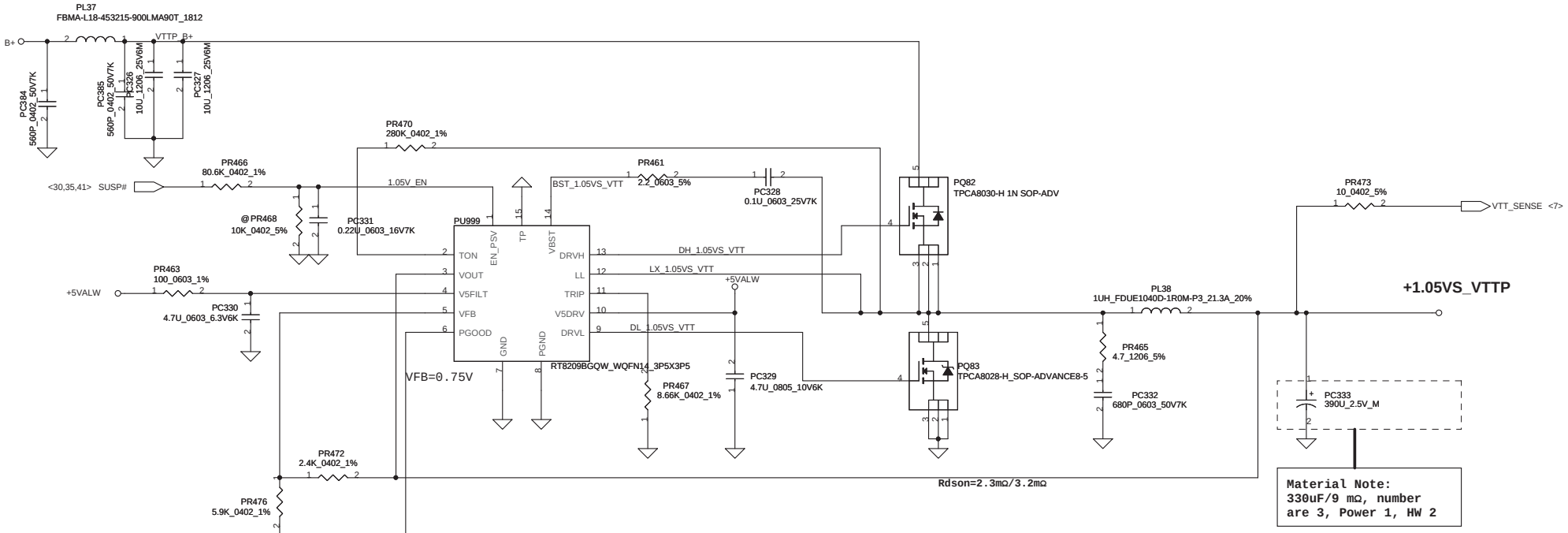

Material Note:
330uF/9 mΩ, number
are 3, Power 1, HW 2

Change from APW7138 to RT8209 at 2010-0428 night.

VFB=0.75V
Vo=VFB*(1+PR308/PR309)=1.05V
Ton=19E-12*Ron*(((2/3)*Vo+100mV)/Vin)+50ns=2.74E-07
Freq=282KHz , 300KHz(typ)

Cesr=15m ohm
Ipeak=19.6A Imax=13.72A Iocp=23.52A
Delta I=((19-1.05)*(1.05/19))/(L*Freq)=1.837A
=>1/2 Delta I=0.918A
Vtrip=Rtrip*10uA=0.0866V
Iocp-min=Vtrip/(Rds(on)(max)*1.2)+1/2 Delta I = 23.471A
Iocp-max=Vtrip/(Rds(on)(typ)*1.2)+1/2 Delta I =32.295A
Iocp=22.4A~30.8A

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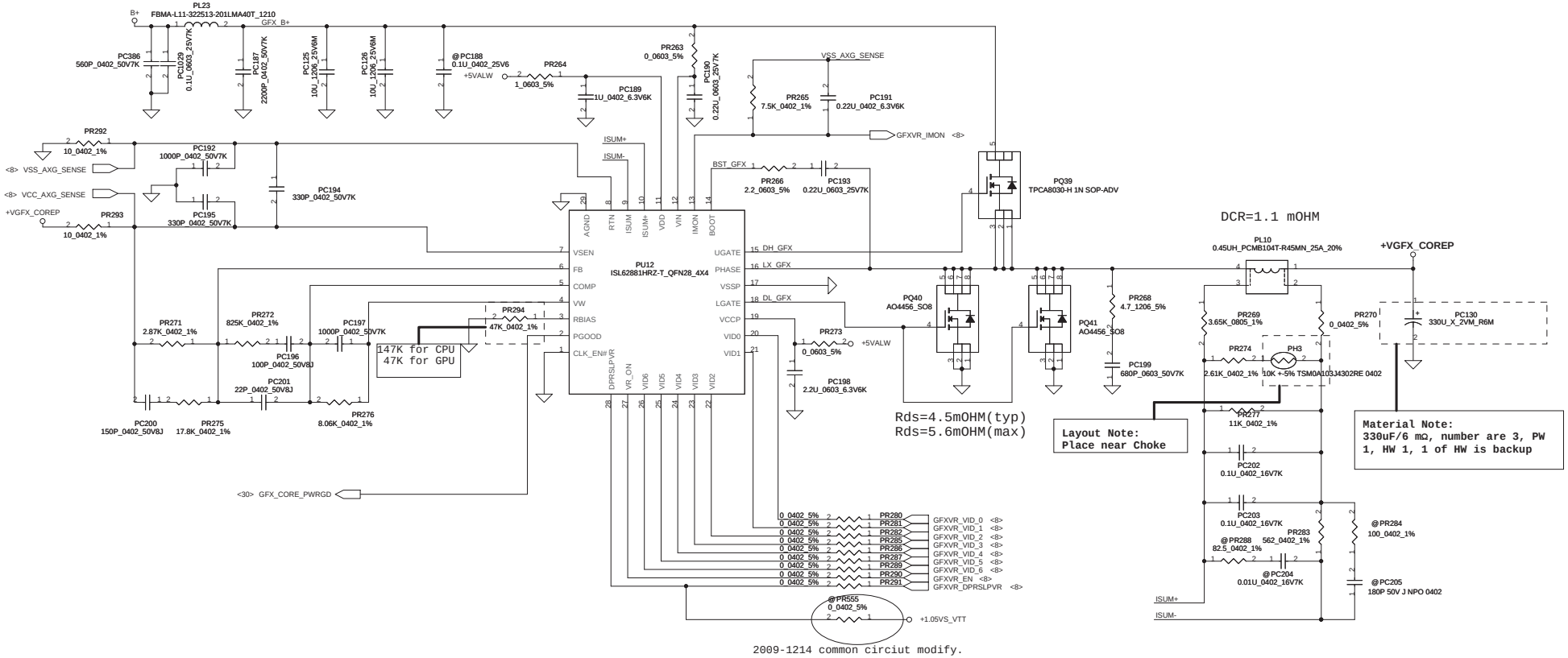
Intel Auburndale CPU(Integrate Graphics) Ipeak=22A Imax=15A
OCP calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum)=0.617
where Rn=PR277 // (PR274+PH3)=5.875k ohm
Rsum=PR269=3.65k ohm
LL=2*Rdroop*G1*DCR/Ri= 6.96m V/A
where Rdroop=PR271=8.66k ohm, Ri=PR283=1.69k ohm
Iocp=OCP Threshold*Rdroop/LL=24.89A



2009-1214 common circiut modify.

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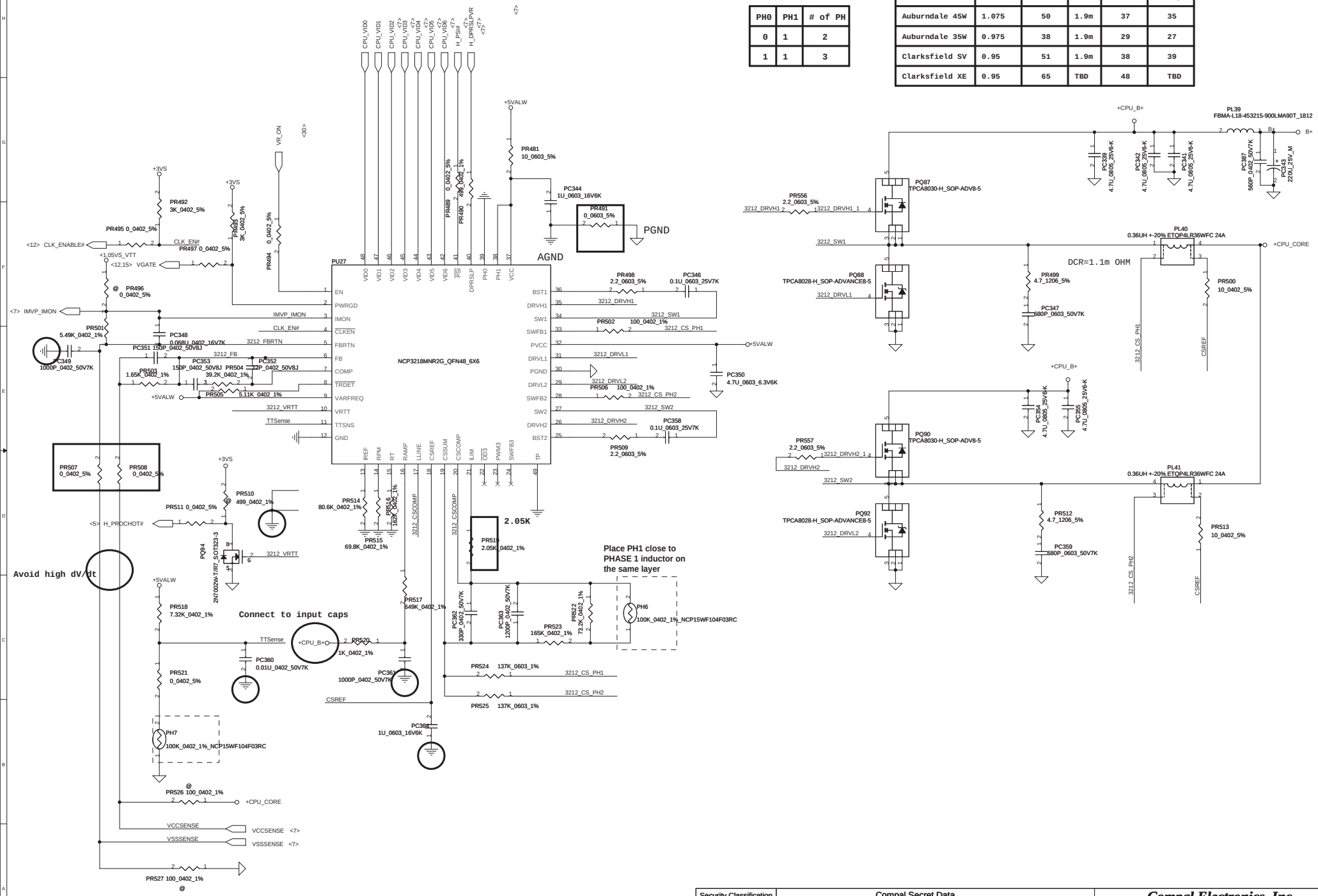
PH0	PH1	# of PH
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD



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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1 2 3	Pre-Charge circiut update.	Pre-Charge circiut disable in EVT, now modify and enable it.	0.1	39	Change PR353 from SD034470280 to SD034200380. Change PR371 from SD034220280 to SD034470280. Change PR587 from SD034100380 to SD034470280. Change PR590 from SD034200280 to SD034143280. Change PR591 from SD028470280 to SD028100380. Add PC1027 SE074222K80(S CER CAP 2200P 0402 50V7K) Change PQ111 from SB000006800 to SB301150200	2010/06/08	to PVT
4	Pre-Charge circiut update.	Pre-Charge circiut disable in EVT, now modify and enable it.	0.1	38	Add PQ102 and PQ103 SB301150200. Add PR592 SD034200380.	2010/06/08	to PVT
5 6	Pre-Charge circiut update.	Pre-Charge circiut disable in EVT, now modify and enable it.	0.1	40	Change PR386 from SD011000080 to SD011100180. Add PR388, PR390, PR391 SD011100180. Add PD14 SC100001Y80 LL4148_LL34-2	2010/06/08	to PVT
7 8	EMI fail, add 3/5V snubber and Boost Resister to silve it.	EMI request to solve EMI issue.	0.1	38	Add PR566 and PR567 SD001470B80 S RES 4.7 1206 5% Add PC1012 and PC1013 SE074681K80 S CER CAP 680P 0402 50V7K Change PR564 and PR565 from SD013000080 to SD013220B80	2010/06/08	to PVT
	EMI fail, add 1.5V snubber.	EMI request to solve EMI issue.	0.1	42	Add PR415 SD001470B80 4.7 1206 5%. Add PC294 SE025681K80 S CER CAP 680P 50V K X7R 0603	2010/06/08	to PVT
9 10	EMI fail, add 1.05V snubber. and Boost Resister.	EMI request to solve EMI issue.	0.1	43	Add PR465 SD001470B80 4.7 1206 5%. Add PC332 SE025681K80 S CER CAP 680P 50V K X7R 0603 Change PR461 from SD013000080 to SD013220B80	2010/06/08	to PVT
11	EMI fail, add GFX_CORE snubber.	EMI request to solve EMI issue.	0.1	44	Add PR268 SD001470B80 4.7 1206 5%. Add PC199 SE025681K80 S CER CAP 680P 50V K X7R 0603	2010/06/08	to PVT
12 13	HW power sequence modify.	HW request.	0.1	43	Change PR466 from SD034576280 S RES 1/16W 57.6K +-1% 0402 to SD034806280 S RES 80.6K 0402 1%) Change PC331 from SE076104K80 S CER CAP .1U 16V K X7R to SE00000R700 S CER CAP 0.22U 16V K X7R 0402	2010/06/08	to PVT
14	BOM unique.	BOM unique.	0.1	38	Chnage PQ101 from SB301150000 to SB301150200.	2010/06/08	to PVT
15	EMI request.	EMI request.	0.1	38	Add PC1028 SE042104K80 S CER CAP .1U 25V K X7R 0603	2010/06/08	to PVT
16	EMI request.	EMI request.	0.1	44	Add PC1029 SE042104K80 S CER CAP .1U 25V K X7R 0603	2010/06/08	to PVT
17	Sourcer request to change a common part.	Sourcer request.	0.1	38	Change PC1019 from SE00000GC00 S CER CAP 2.2U 10V K X7R 0603 to SE000003H00 S CER CAP 2.2UF 10V K X5R 0603	2010/06/08	to PVT
18	Per sourcer request.	Sourcer request to change PC331 from SE00000R700 to SE026224K80 for common part.	0.1	43	change PC331 from SE00000R700 to SE026224K80	2010/06/08	to PVT
19	CPU transient issue.	Need modify PC362 to 330P due to transient fail.	0.1	45	Change PC362 from SE074561K80 S CER CAP 560P 50V K X7R 0402 to SE074331K80 S CER CAP 330P 50V K X7R 0402	2010/06/08	to PVT
20	Per sourcer request.	Per sourcer request.	0.1	43 44	Chnage PQ39/PQ82 from SB000008L80 to SB00000HL00.	2010/06/08	to PVT
21	Cost down.	Cost down 3VALWP and Charger Low Side MOS.	0.1	38 39	Change PQ98 from SB00000AJ00 to SB000009580(AO4468). Change PQ64 from SB00000CG00 to SB000009580(AO4468).	2010/06/08	to PVT
22	Cost down.	Cost down +1.5VP Low side MOS and choke.	0.1	42	Chnage PQ74 from SB000009F80 to SB00000AJ00(AO4712). CHnage PL32 from SH000009U00 to SH000009680.	2010/06/08	to PVT
23	Cost down.	re-caculate 1.5VP OCP.	0.1	42	Change PR417 from SD034110280 to SD034182280.	2010/06/08	to PVT

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	Cost down.	re-caculate +3VALWP OCP.	0.1	38	Change PR562 from SD034107380 to SD034137380.	2010/06/08	to PVT
25							
26							
27							
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Version change list (P.I.R. List)

Item	Phase	PAGE	DATE	Modifycatio list	Purpose
1	EVT		04 / 08	N/A	
			04 / 16	Modify RTC SCH Change LAN to AR8152 Update Power SCH	
			04 / 21	Update AND Gate symbol - U1 / U2 / U6 / U7 / U19 Update Power MOS symbol - U24 / U25 / U26 C196 change to 1U for INTEL disign CLK GEN del C35 / C36 / C30 / C31 / C32 / C33 / C34 / L3 (for 3G@ and @ function) Q4+Q6 change to 2N7002DW Update U8 symbol Add DMIC function Modify USB define.	
			04 / 26	Update Power SCH	
			04 / 27	Add R17 for DMIC power	
			04 / 29	Update Power SCH Change LAN to GIGA&10/100 co-lay Del R307 (LVDS conn.) Change +1.05VS_VTT to +1.05VS (CLK GEN) Change C842 / C850 / C854 / C656 to SE080105K80 1U_0603_10V6K Change R940 to 28K (S3 Power sequence)	
			04 / 29	SW T1 pin define (LAN)	
			05 / 03	Change R907 (0_0603) to 0_1206 5% Remove C40 / C41 / C42 / C43 / C44 Change FAN Conn.	
			05 / 03	Update Power SCH Change LAN to BCM57780 GIGA	
			05 / 06	Del R637 / R639 / R640 / R645 / R647 / R648 (AUDIO) Del DMIC Update Power SCH	
			05 / 07	Update Power SCH Add C49 / C50 (EC B+)	
			05 / 10	Update Power SCH	
			05 / 11	C764 / C765 change to 18P_0402_50V8J (EC) Reserve D13 / D24 / D30 (ESD)	
			05 / 12	U17 change to RTS5137 (SA000043500) Card reader	
			05 / 13	Update Power SCH	
			06 / 01	Unpop L11 / C247 & Pop R304 for cost down Unpop C764 / X2 & Pop R13 & C765 Change to 100K for EC remove Crystal Pop R834 & R835 change to 200K for Project ID	
			06 / 02	Unpop D24 / D30 Unpop R690 / R691 Pop C49 / C50 For HDMI Unpop R753 / R757 , Add R754 / R758 to 0 ohm. Change R759 to 3.9K. Change R755 to 4.7K ohm , Unpop R748. Unpop R778. R833 / R292 0_0805 change to 0_0603.	
			06 / 03	C190 / C191 & C1135 / C1136 change to 33P 0402 50V8J for Vender test report	
			06 / 04	Unpop C774~C799 for EMI cost down. Update Power SCH	
			06 / 10	Add T25 / T26 / T27	

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